

In The Name Of Allah

Chapter 6
Introduction to Sequential Devices

Department of Electrical Engineering

Islamic Azad University

Qazvin Branch

The Sequential Circuit Model

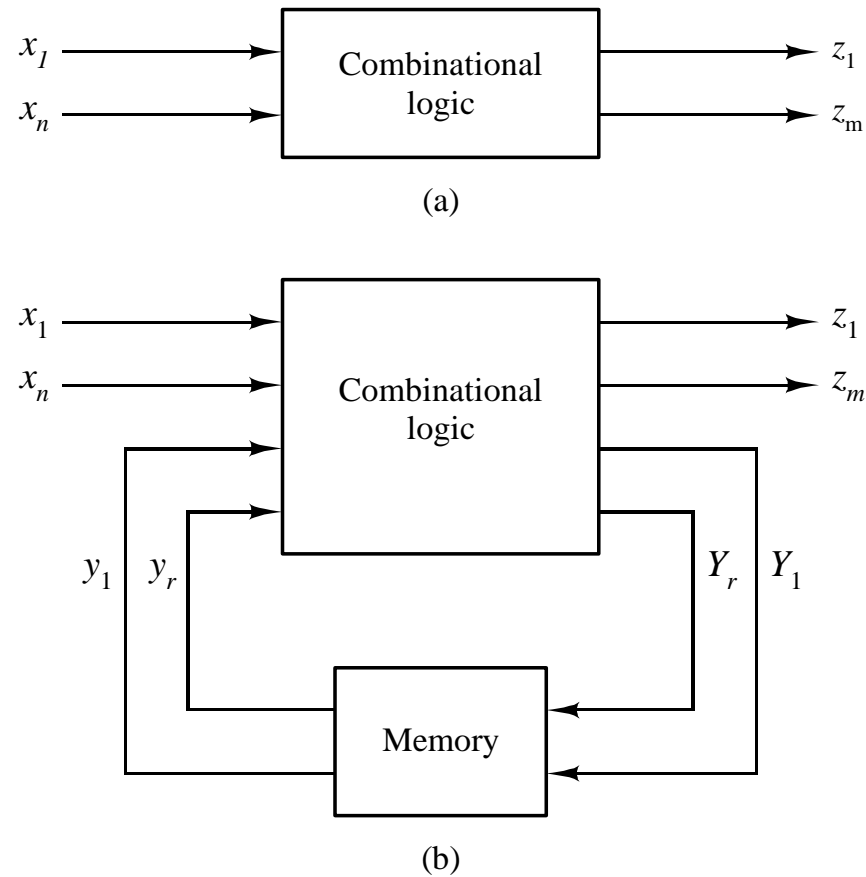


Figure 6.1

State Tables and State Diagrams

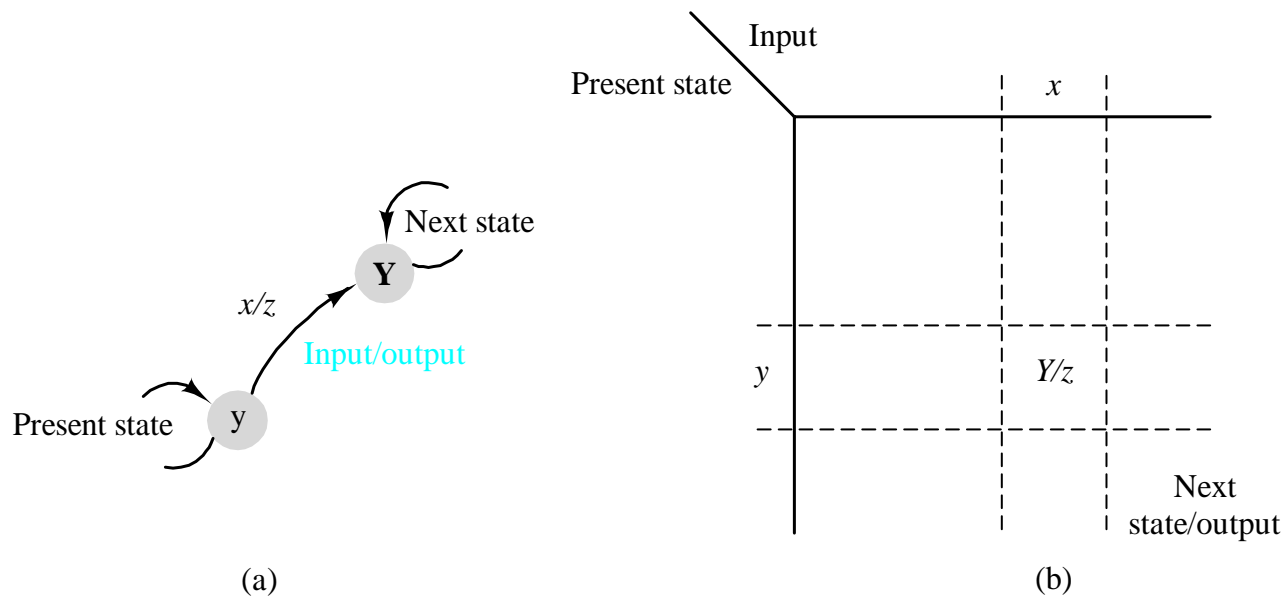


Figure 6.2

Sequential Circuit Example

		Input x	
		0	1
Present state	A	D/0	C/1
	B	B/1	A/0
	C	C/1	D/0
	D	A/0	B/1

(a)

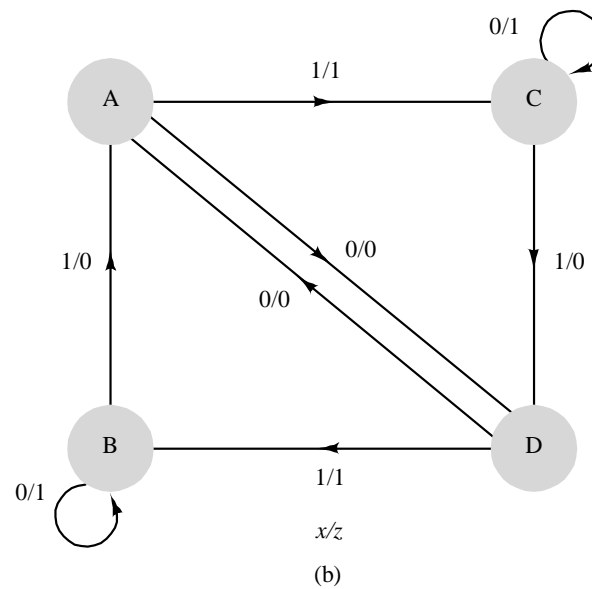


Figure 6.3

Latch and Flip-flop Timing

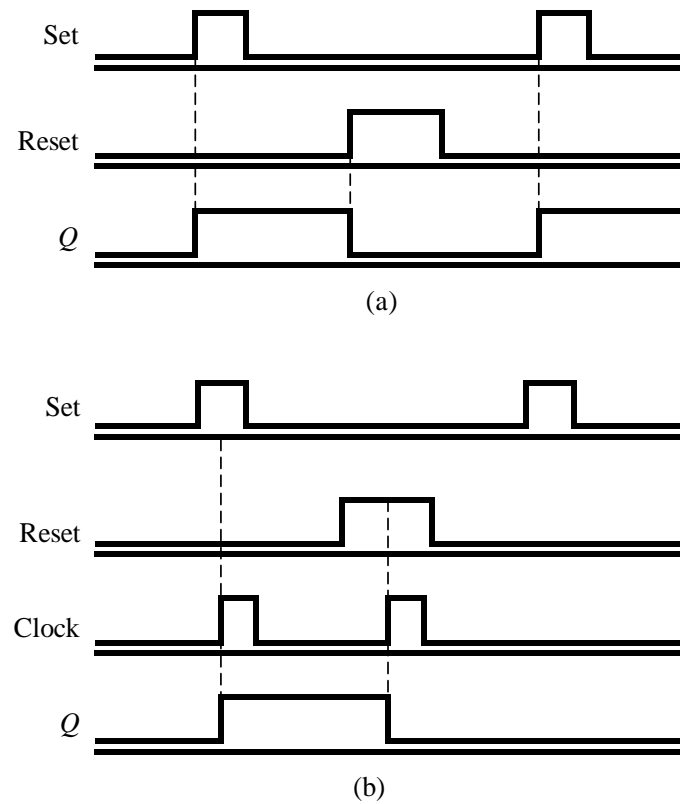


Figure 6.4

TTL Memory Elements

TABLE 6.1 TTL MEMORY ELEMENTS [1]

Device	Number of Elements	Element Description
74LS73A	2	Negative-edge triggered JK flip-flop with clear
7474	2	Positive-edge-triggered D flip-flop with preset and clear
74LS75	4	D latch with enable
7476	2	Pulse-triggered JK flip-flop with preset and clear
74111	2	Master-slave JK flip-flop with preset, clear, and data lockout
74116	2	4-Bit hazard-free D latch with clear and dual enable
74175	4	Positive-edge triggered D flip-flop with clear
74273	8	Positive-edge triggered D flip-flop with clear
74276	4	Negative-edge triggered JK flip-flop with preset and clear
74279	4	SR latch with active-low inputs

6.3 Latches

➤ Set Latch

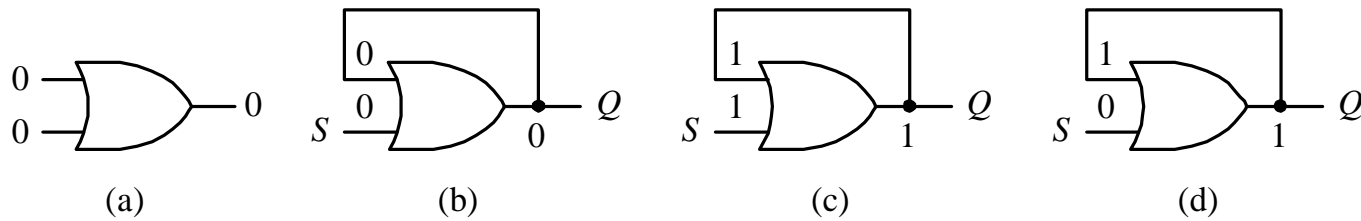


Figure 6.5

6.3 Latches

➤ Reset Latch

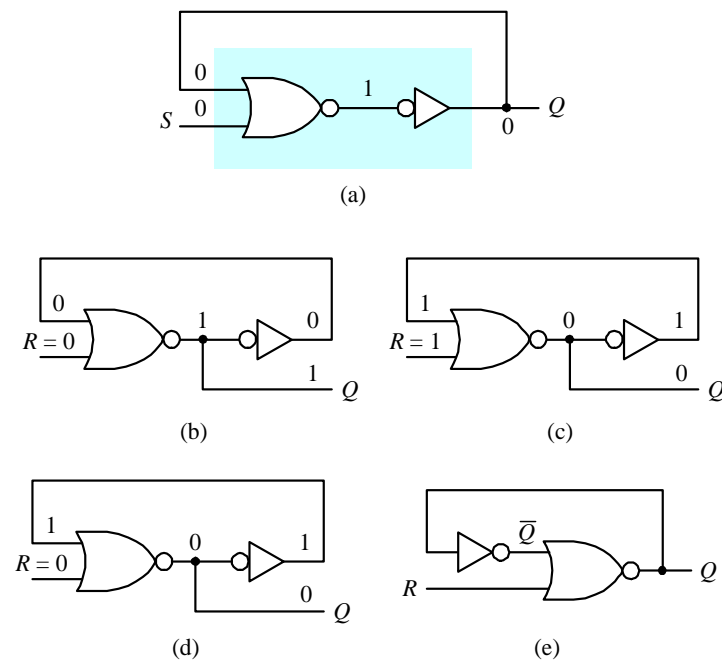


Figure 6.6

6.3 Latches

➤ Set-Reset Latch (SR latch)

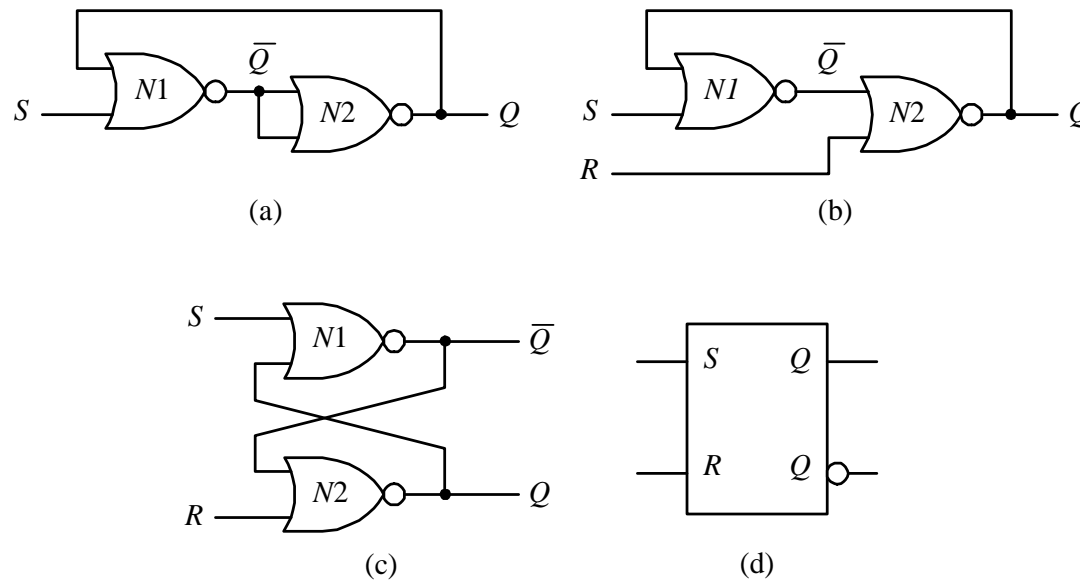


Figure 6.7

6.3 Latches

➤ NAND SR Latch

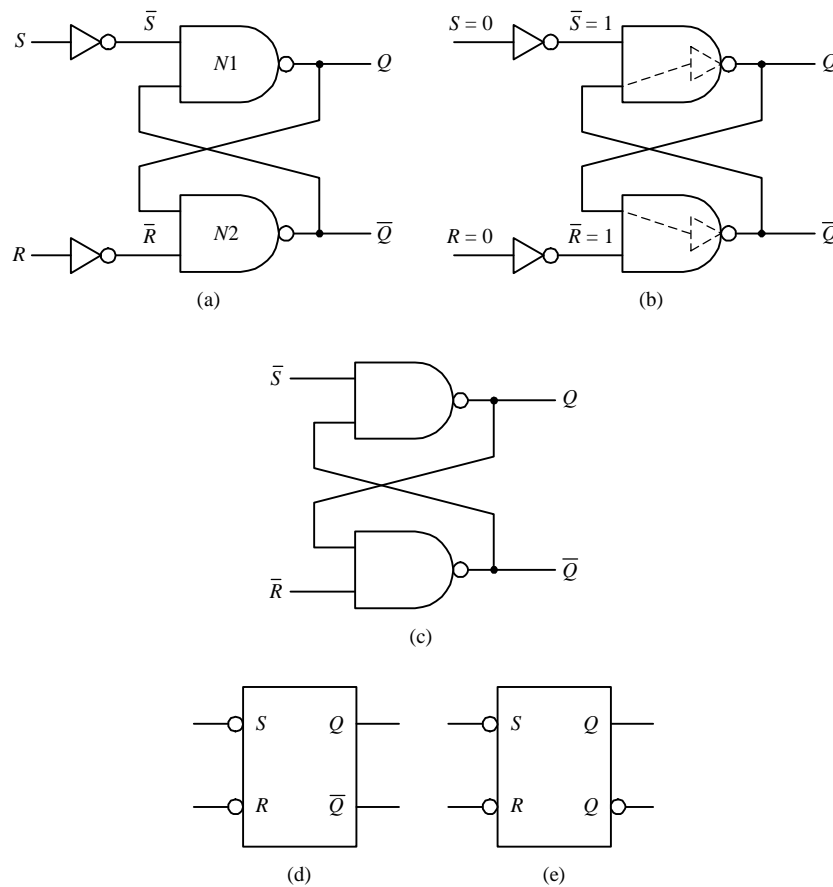
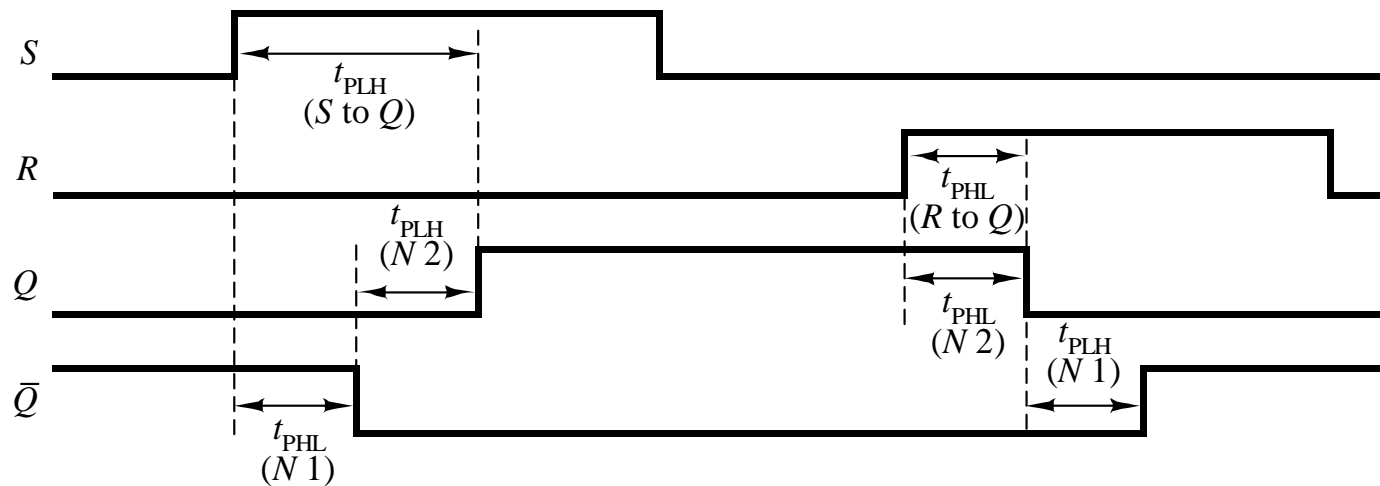


Figure 6.8

6.3 Latches

➤ SR Latch Propagation Delays



6.3 Latches

➤ SR Latch Characteristics

Excitation inputs		Present state	Next state	
<i>S</i>	<i>R</i>	<i>Q</i>	<i>Q*</i>	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	×	Not allowed
1	1	1	×	

(a)

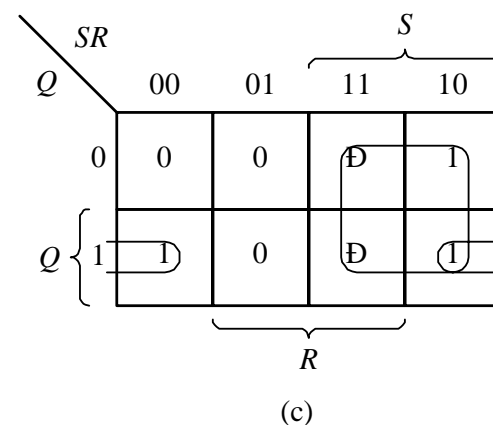
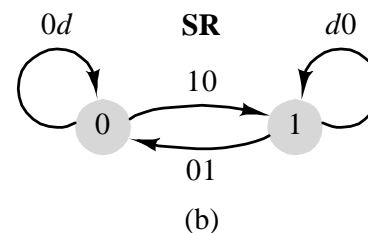


Figure 6.11

$$Q^* = S + R'Q$$

6.3 Latches

➤ SN74279 Latch with Two Set Inputs

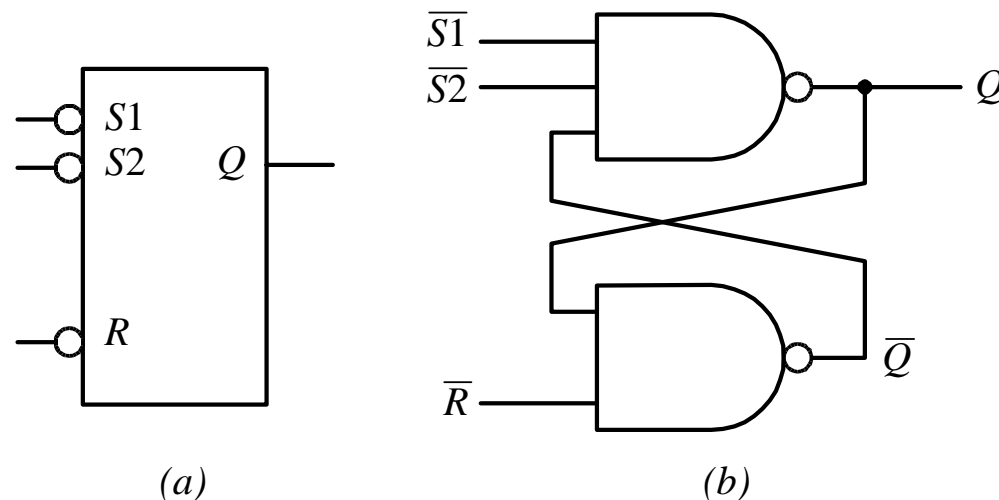


Figure 6.12

6.3.2 Gated SR Latch

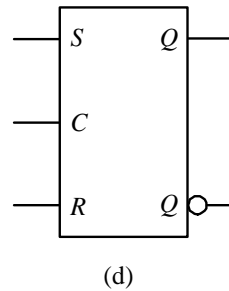
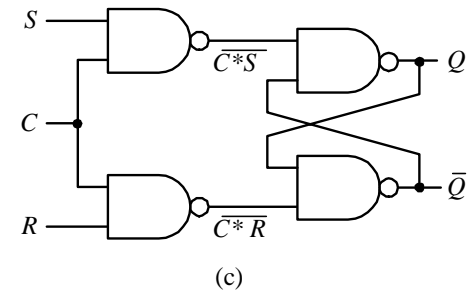
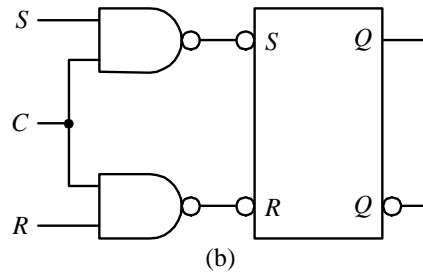
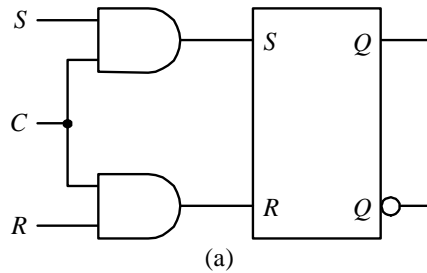


Figure 6.13

6.3.2 Gated SR Latch

➤ Gated SR Latch Characteristics

Enable inputs C	Excitation inputs		Present state Q	Next state Q^*	
	S	R			
0	×	×	0	0	Hold
0	✓	✓	1	1	
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	×	Not allowed
1	1	1	1	×	

(a)

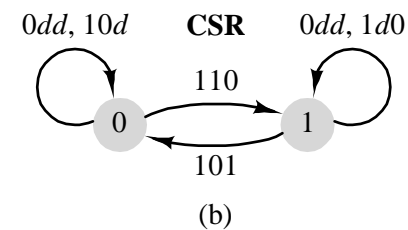


Figure 6.14

$$Q^* = SC + R'Q + C'Q$$

6.3.3 Delay Latch (D latch)

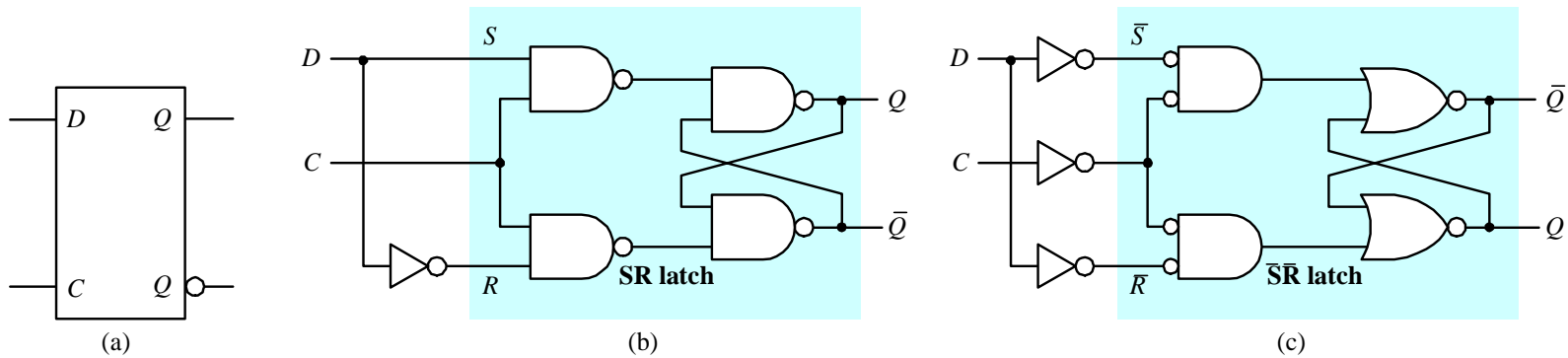


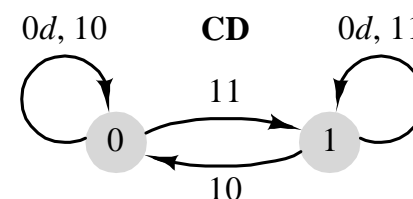
Figure 6.15

6.3.3 Delay Latch (D latch)

➤ D Latch Characteristic

Enable input C	Excitation input D	Present state Q	Next state Q^*	
0	×	0	0	Hold
0	′	1	1	
1	0	0	0	Store 0
1	0	1	0	
1	1	0	1	Store 1
1	1	1	1	

(a)



(b)

Figure 6.16

$$Q^* = DC + C'Q$$

6.3.3 Delay Latch (D latch) D Latch Timing Diagram

➤ D Latch Timing Diagram

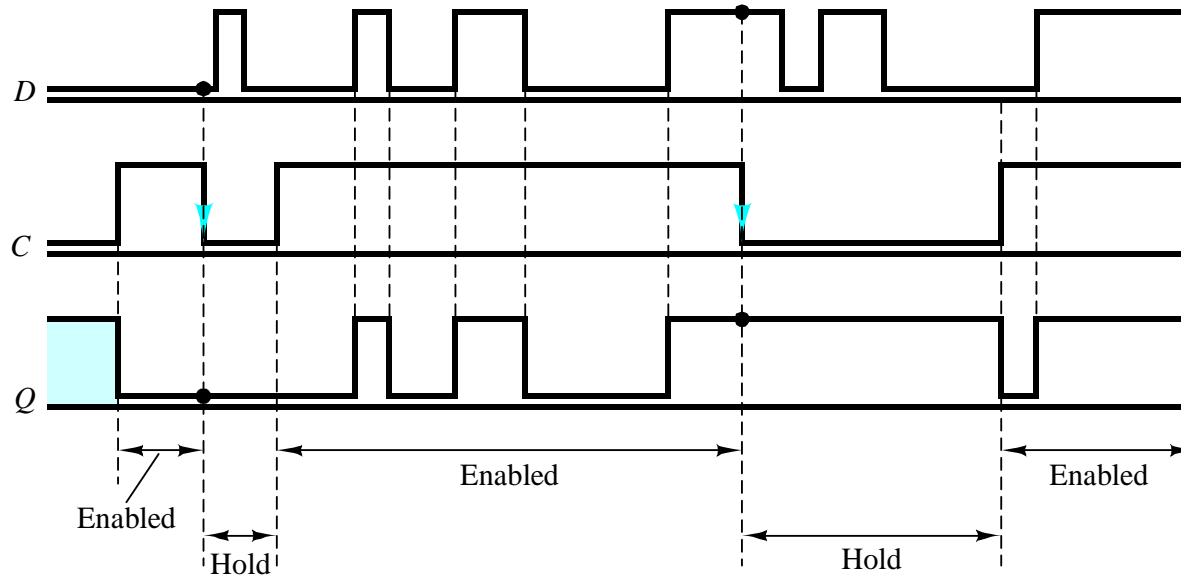


Figure 6.17

6.3.3 Delay Latch (D latch)

➤ D Latch Timing Constraints

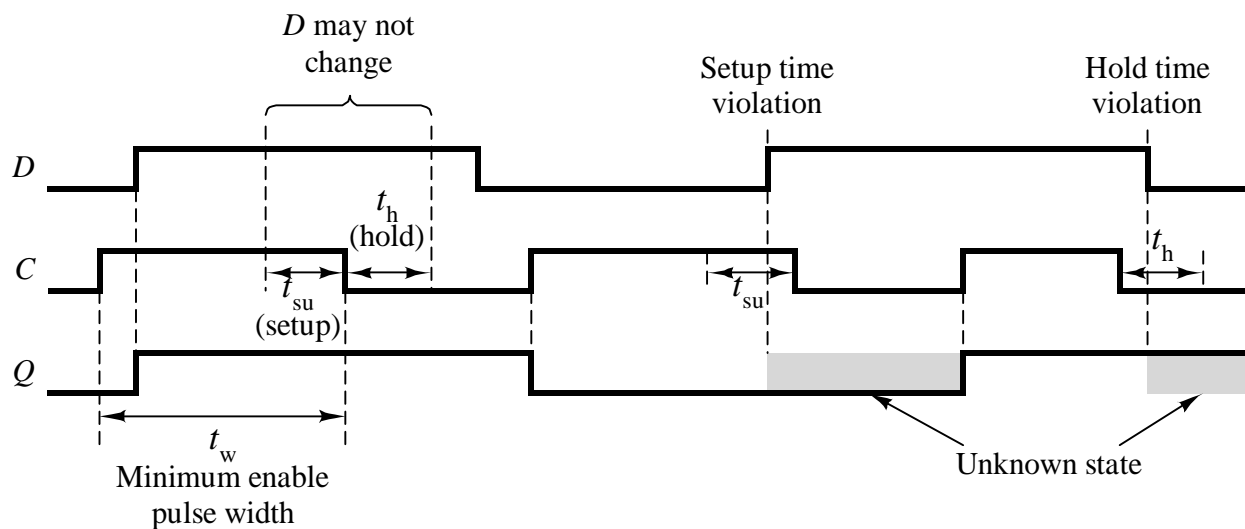


Figure 6.18

6.3.3 Delay Latch (D latch)

➤ The SN74LS75 D Latch

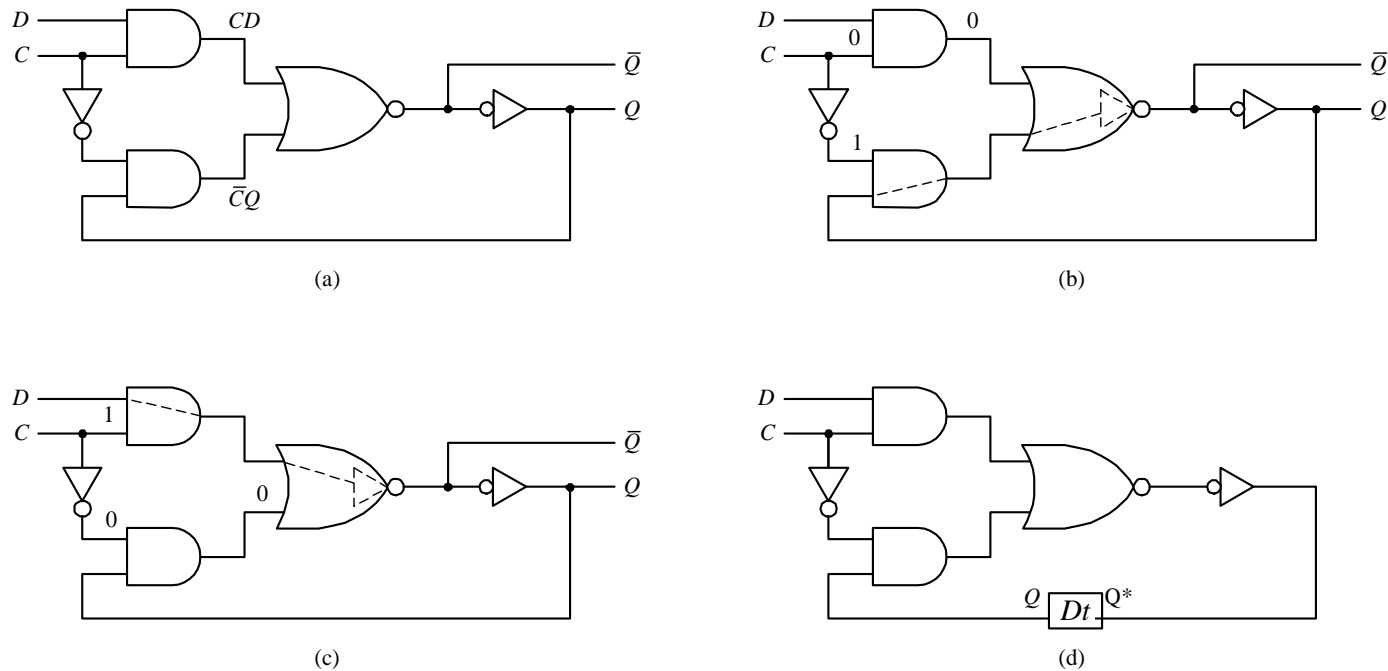


Figure 6.19

6.3.3 Delay Latch (D latch)

➤ Propagation Delays and Time Constraints for the SN74LS75

TABLE 6.2 PROPAGATION DELAYS AND TIME CONSTRAINTS FOR THE SN74LS75 [1]

Timing Parameter	Typical Value (ns)
$t_{PLH} (D \rightarrow Q)$	15
$t_{PIL} (D \rightarrow Q)$	9
$t_{PHL} (D \rightarrow \bar{Q})$	12
$t_{TFL} (D \rightarrow \bar{Q})$	7
$t_{PLH} (C \rightarrow Q)$	15
$t_{PIL} (C \rightarrow Q)$	14
$t_{PLH} (C \rightarrow \bar{Q})$	16
$t_{PHL} (C \rightarrow \bar{Q})$	7
t_{su} (minimum setup time for D)	20
t_h (minimum hold time for D)	5
t_w (minimum pulse width on C)	20

6.3.3 Delay Latch (D latch)

➤ Hazard-Free D Latch, the SN74116

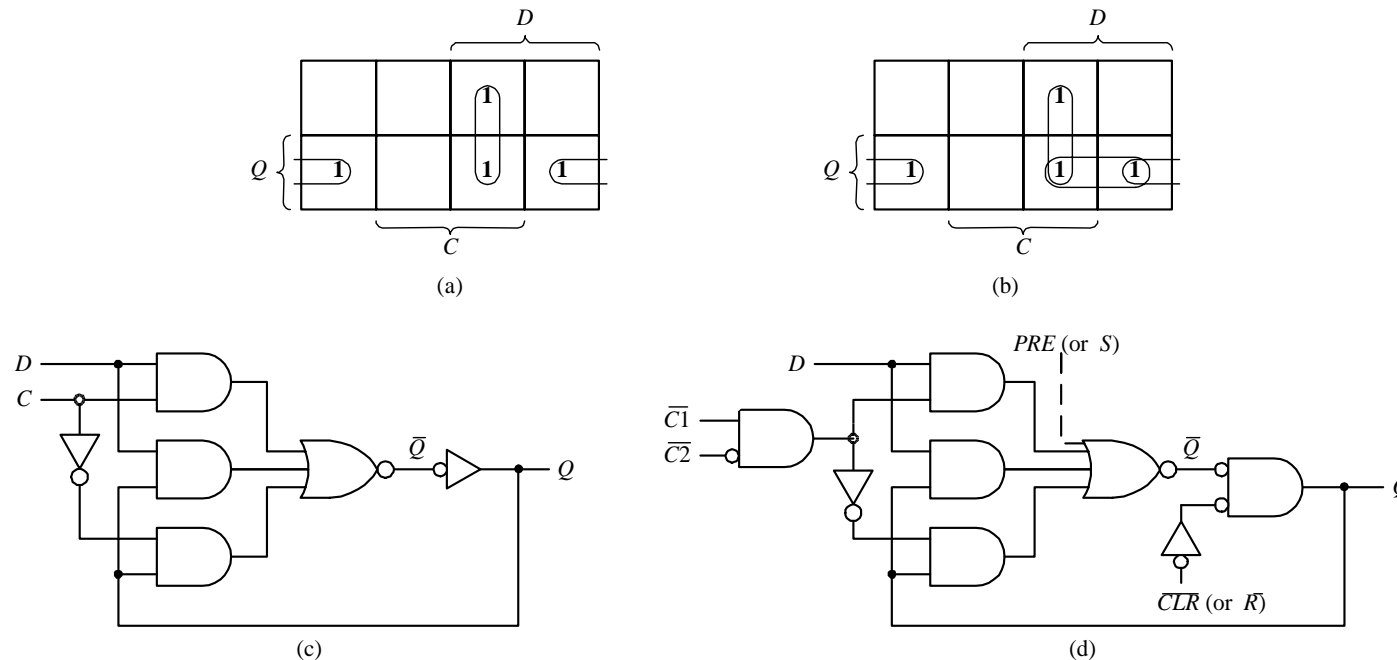


Figure 6.20

$$Q^* = DC + C'Q + DC$$

6.4 Flip-Flops

➤ 6.4.1 Master-Slave SR Flip-flop

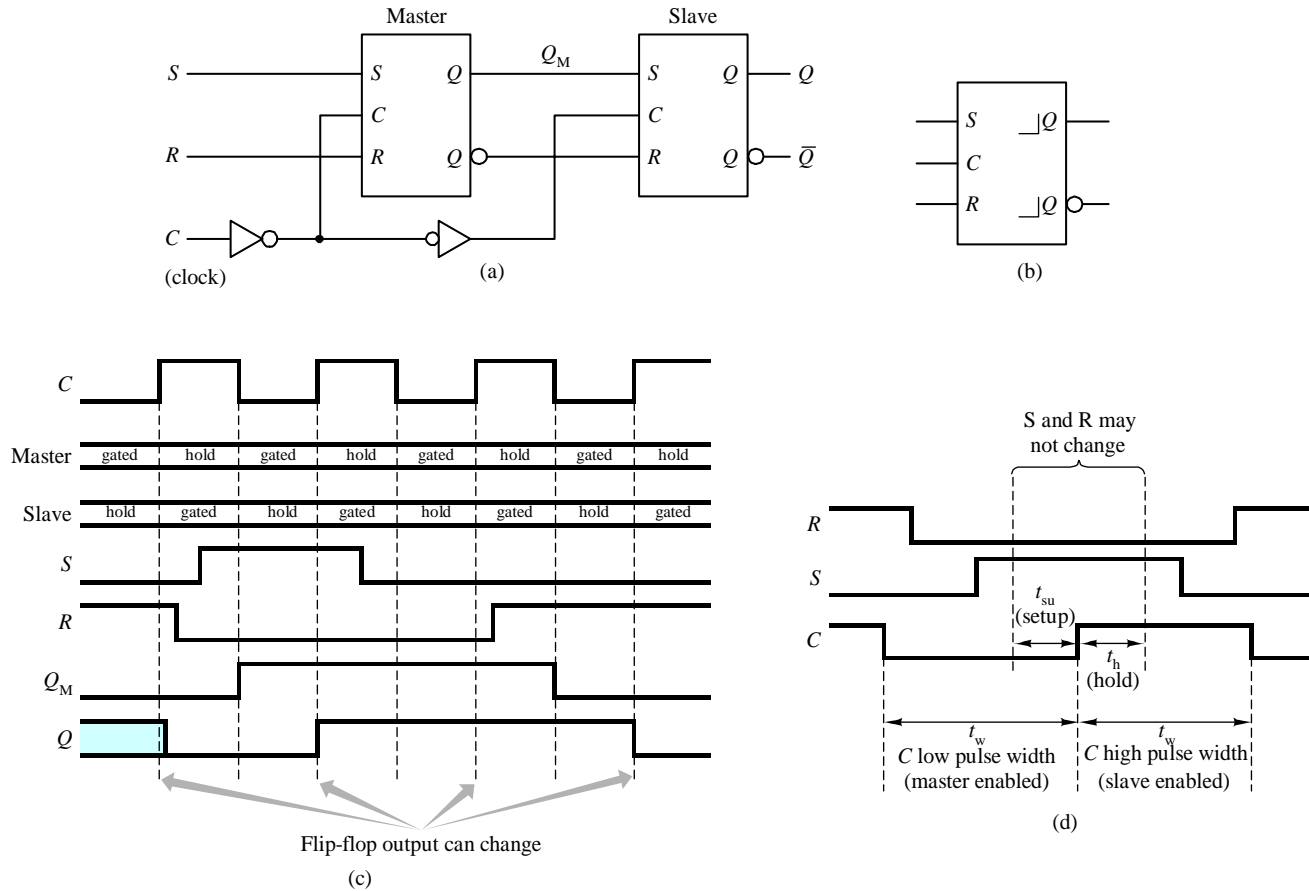







Figure 6.20

6.4 Flip-Flops

➤ SR Master-Slave Flip-Flop Characteristics

S	R	Q	C	Q^*
0	0	0		0 No change
0	0	1		1
0	1	0		0 Reset
0	1	1		0
1	0	0		1 Set
1	0	1		1
1	1	0		× Not allowed
1	1	1		×

(a)

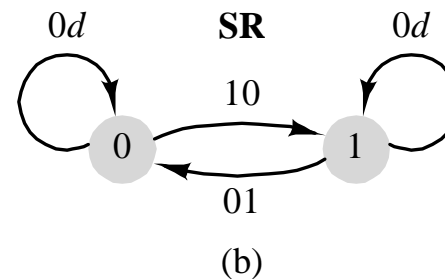


Figure 6.22

$$Q^* = S + R'Q$$

6.4 Flip-Flops

➤ 6.4.2 Master-Slave D Flip-Flop

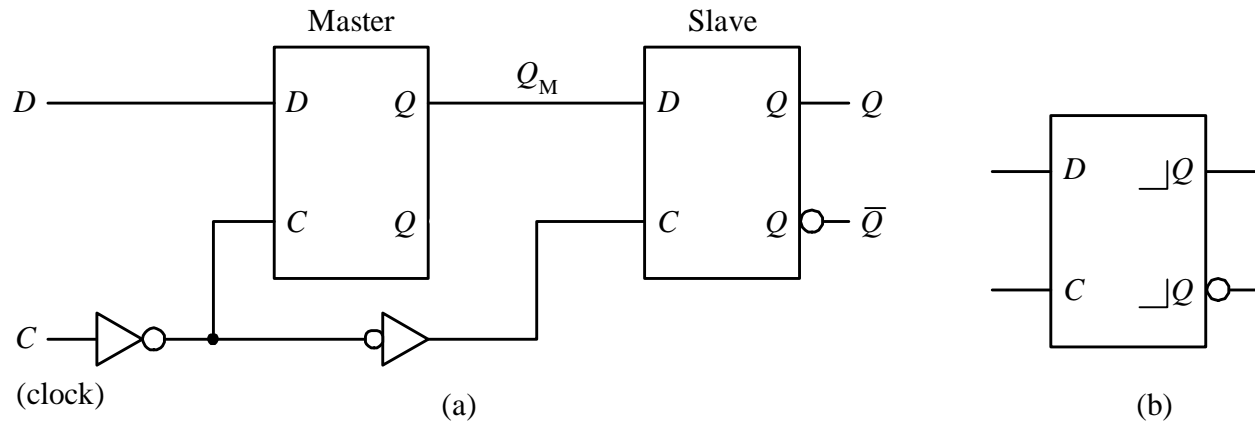


Figure 6.23

6.4 Flip-Flops

➤ Master-Slave D Flip-Flop Characteristics

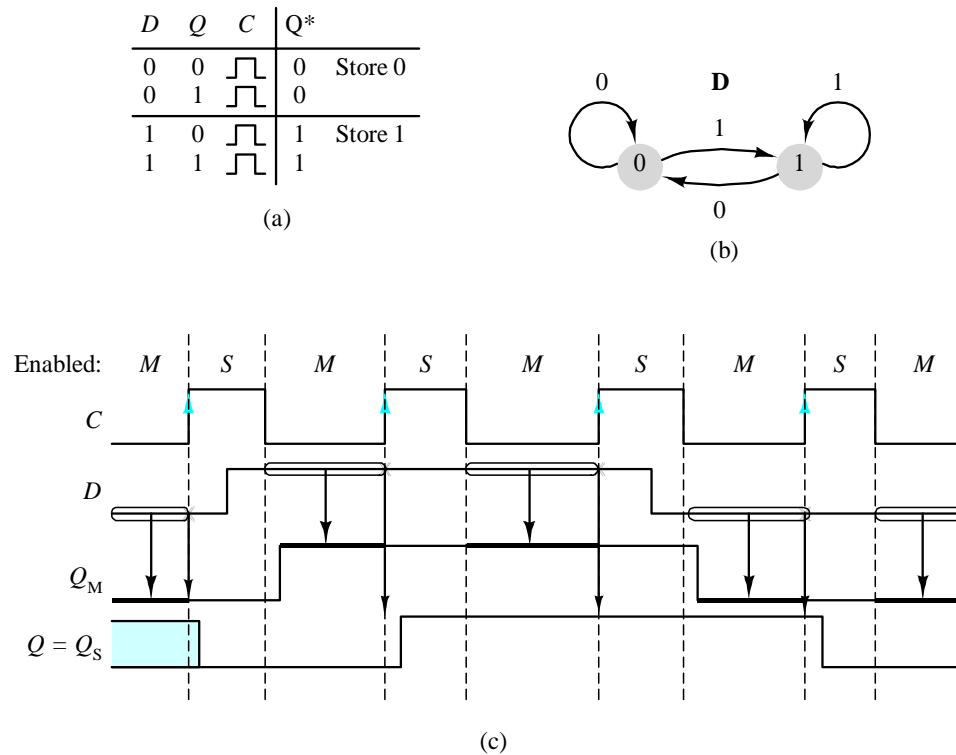


Figure 6.24

$$Q^* = D$$

6.4 Flip-Flops

➤ Pulse-Triggered JK Flip-Flop Characteristics

J	K	Q	C	Q^*
0	0	0		0 Hold
0	0	1		1
0	1	0		0 Reset
0	1	1		0
1	0	0		1 Set
1	0	1		1
1	1	0		1 Toggle
1	1	1		0

(a)

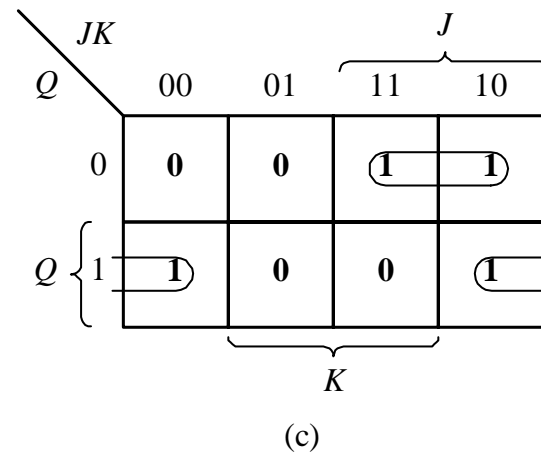
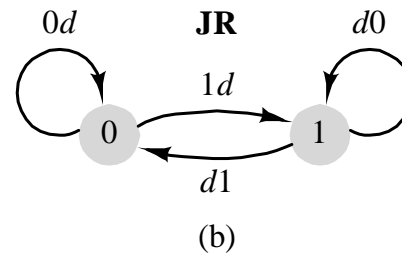


Figure 6.25

$$Q^* = K'Q + JQ'$$

6.4 Flip-Flops

➤ Pulse-Triggered JK Flip Realization

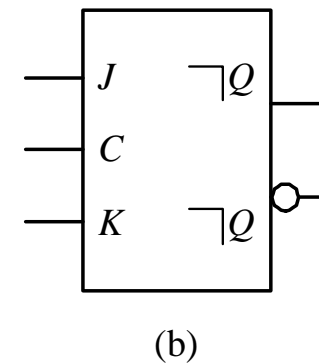
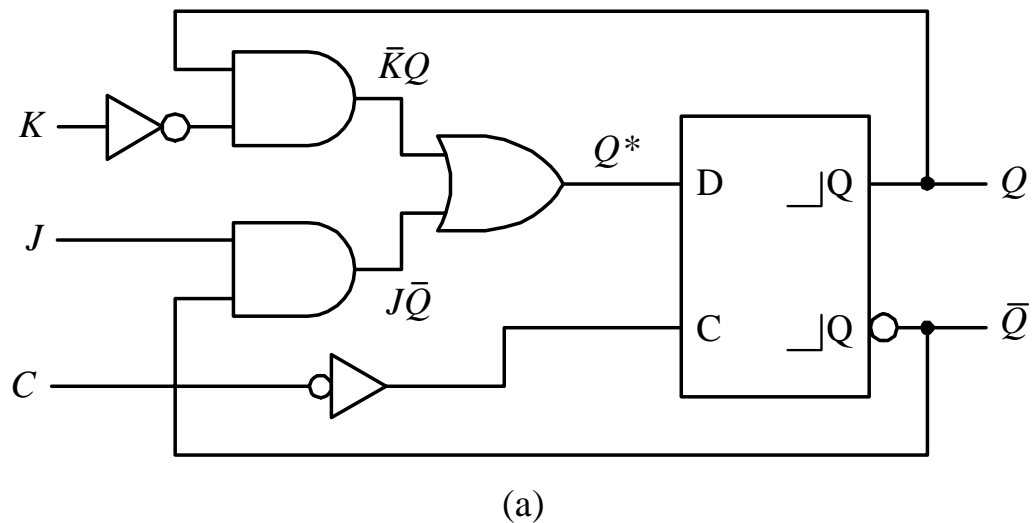


Figure 6.26

6.4 Flip-Flops

➤ The SN7476 Dual Pulse-Triggered JK Flip-Flop

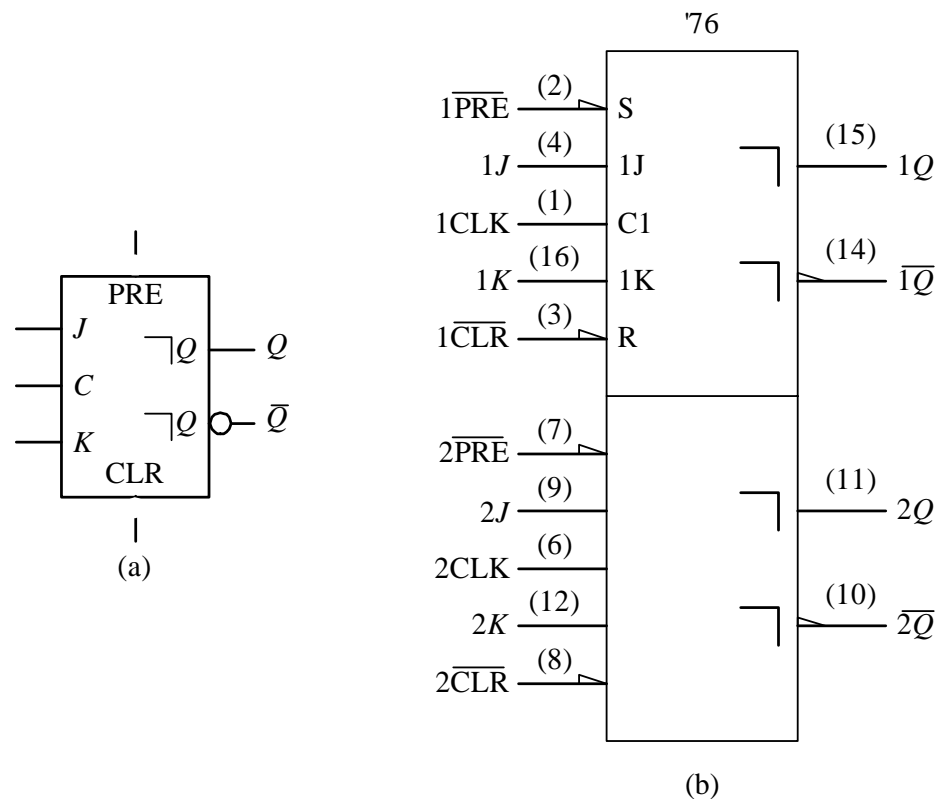


Figure 6.27

6.4 Flip-Flops

➤ SN7474 Dual Positive-Edge-Triggered D Flip-Flop

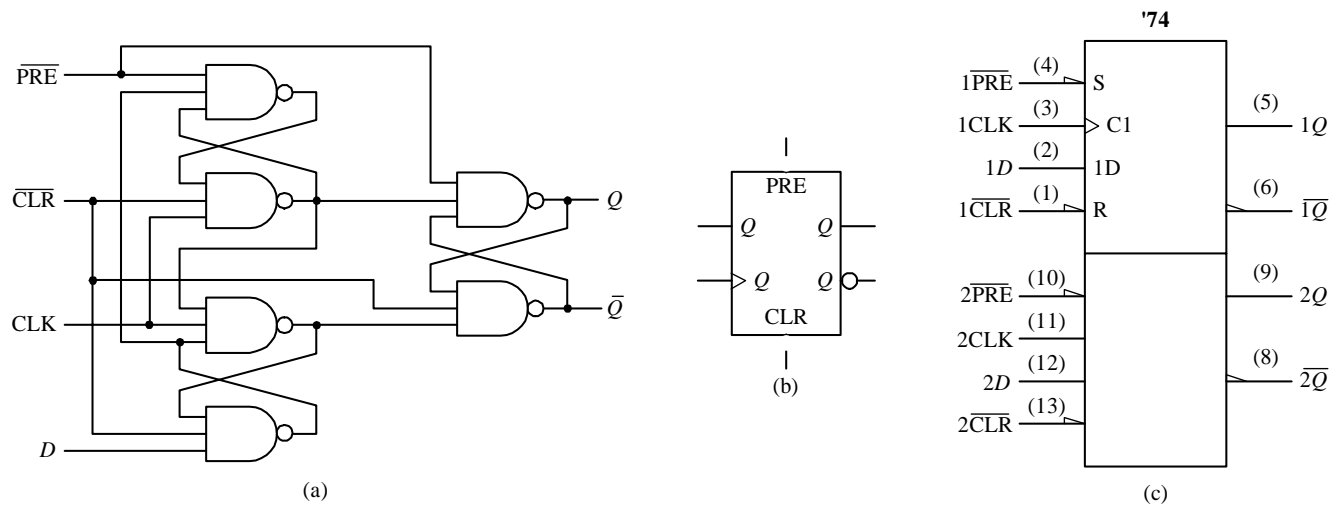


Figure 6.28

6.4 Flip-Flops

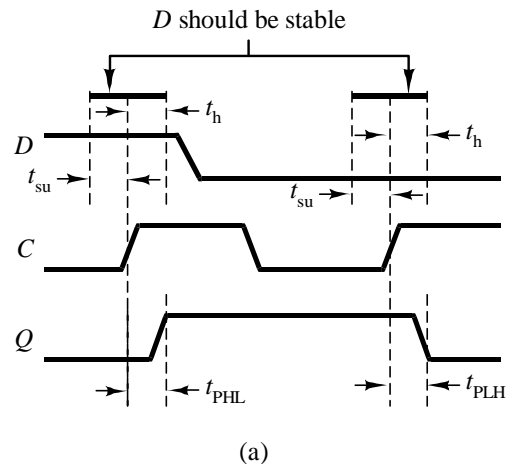
➤ SN7474 Excitation Table

Inputs				Outputs		Mode
\overline{PRE}	\overline{CLR}	D	CLK	Q	\overline{Q}	
L	H	×	×	H	L	Set
H	L	×	×	L	H	Clear
L	L	×	×	H	H	Not allowed
H	H	H	↑	H	L	Clocked operation
H	H	L	↑	L	H	Clocked operation
H	H	×	L	Q_0	\overline{Q}_0	Hold

Figure 6.29

6.4 Flip-Flops

➤ SN7474 Flip-Flop Timing Specifications



To Output Q from:	Delay Parameter	Value (ns)
Clock	t_{PLH}	25
	t_{PHL}	40
PRE	t_{PLH}	25
	t_{PHL}	40
CLR	t_{PLH}	25
	t_{PHL}	40

(b)

Input Pin	Constraint	Minimum Value (ns)
D	t_{su}	20
D	t_h	5
Clock	t_w low	30
Clock	t_w high	37
CLR	t_w low	30
PRE	t_w low	30

(c)

Figure 6.30

6.4 Flip-Flops

➤ SN74175 Positive-Edge-Triggered D Flip-Flop

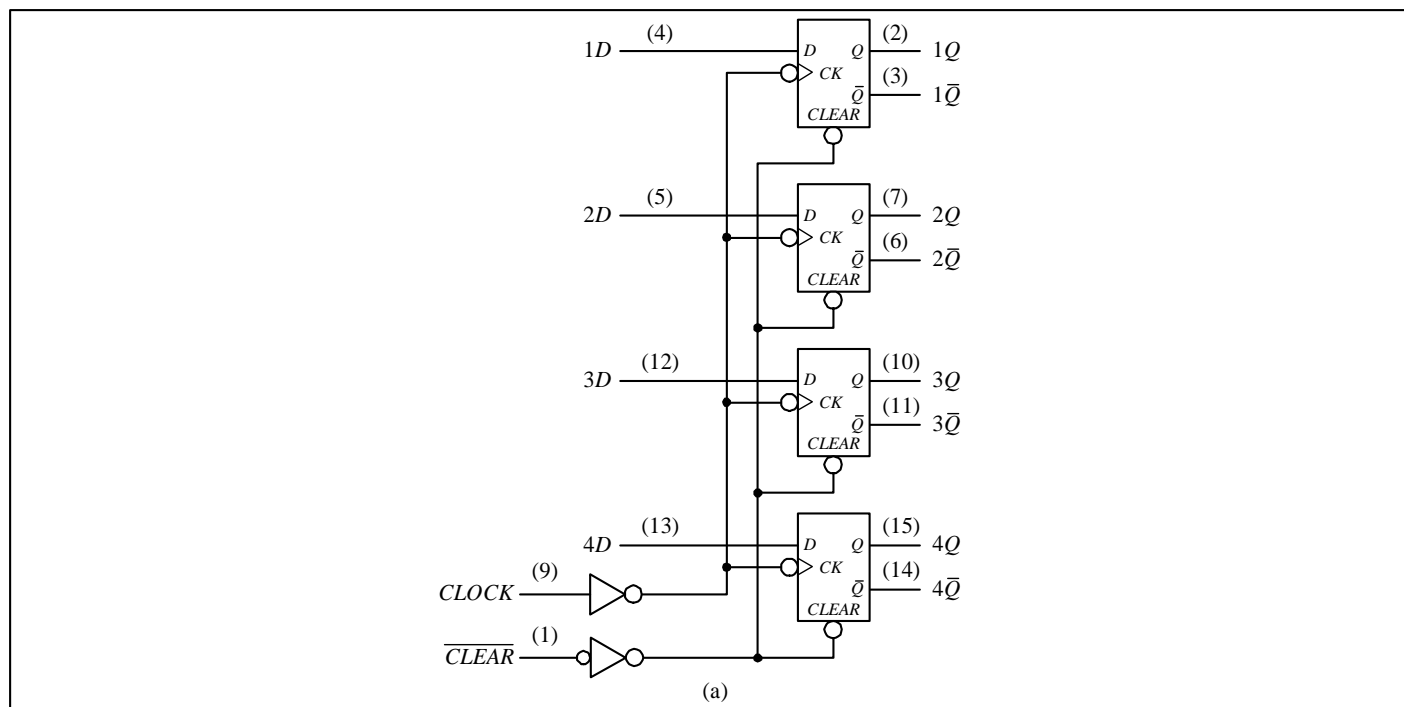


Figure 6.31 (a)

6.4 Flip-Flops

➤ SN74273 Positive-Edge-Triggered D Flip-Flop

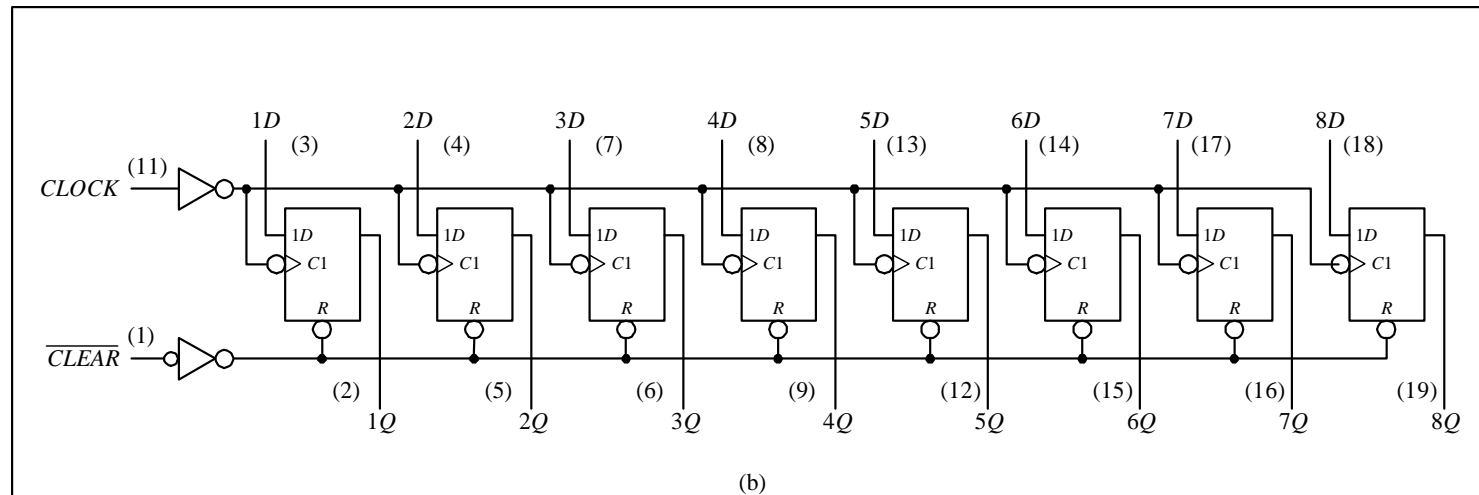


Figure 6.31 (b)

6.4 Flip-Flops

➤ SN74LS73A Edge-Triggered JK Flip-Flop Logic Diagram

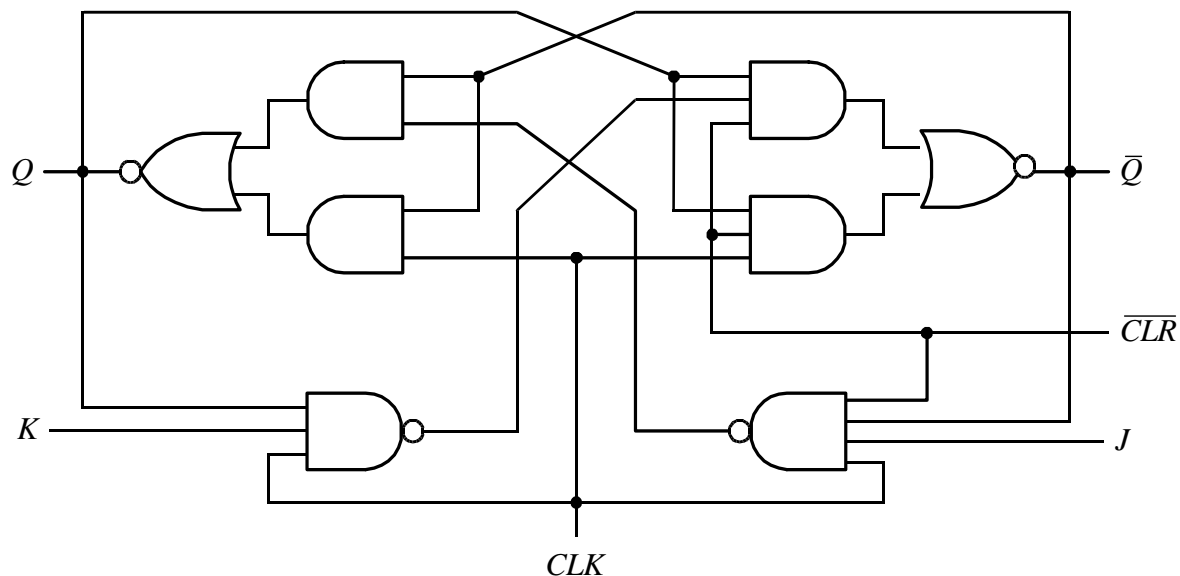


Figure 6.32 (a)

6.4 Flip-Flops

➤ SN74LS73A Logic Symbols

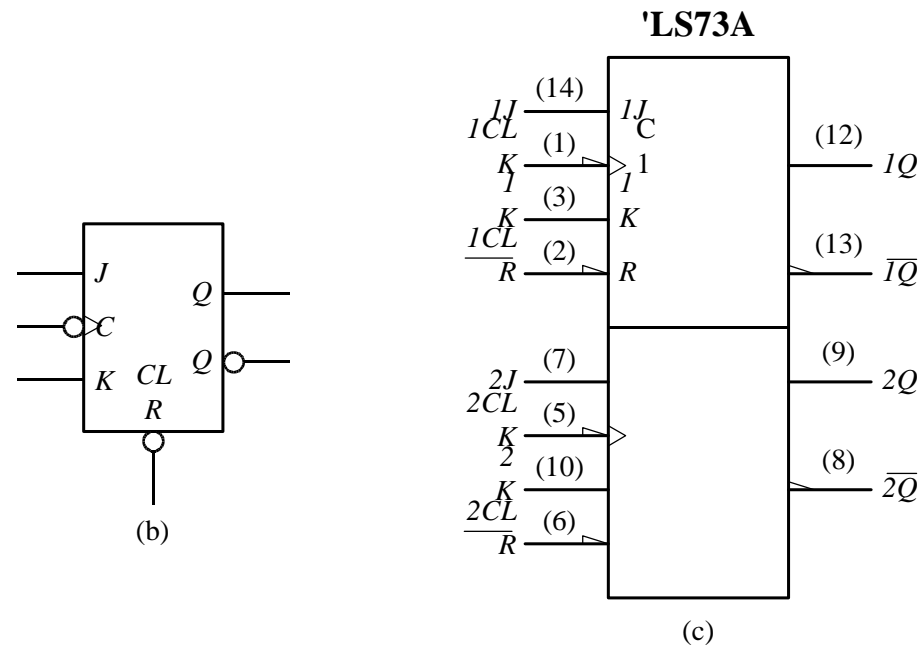


Figure 6.32 (b) and (c)

6.4 Flip-Flops

➤ SN74276 and SN74111 Edge-Triggered K Flip-Flops

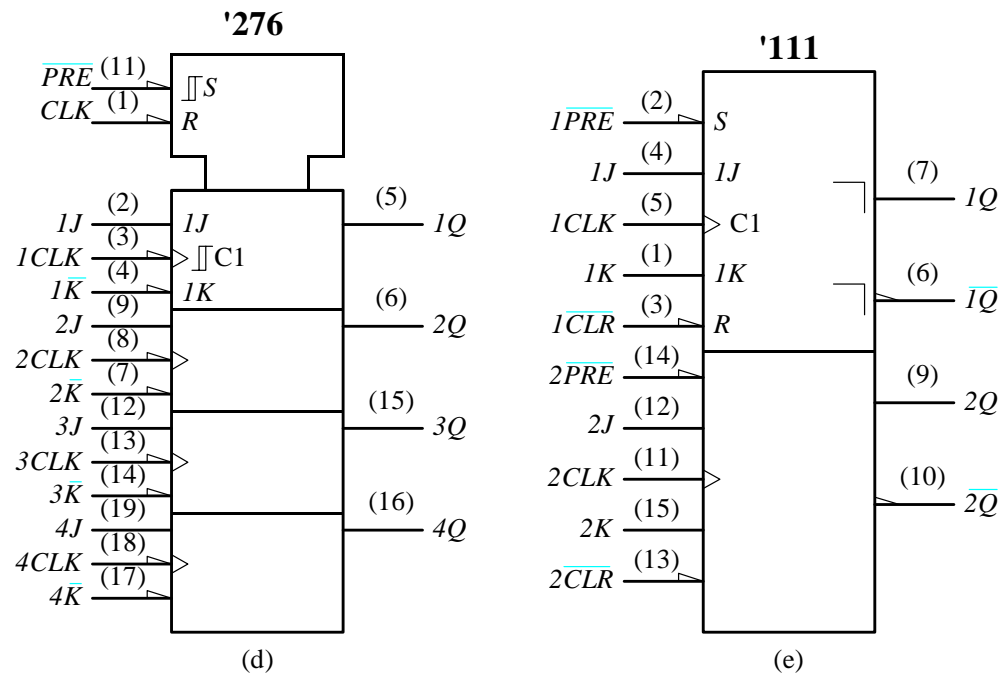


Figure 6.32 (d) and (e)

6.4 Flip-Flops

➤ Negative-Edge-Triggered T Flip-Flop

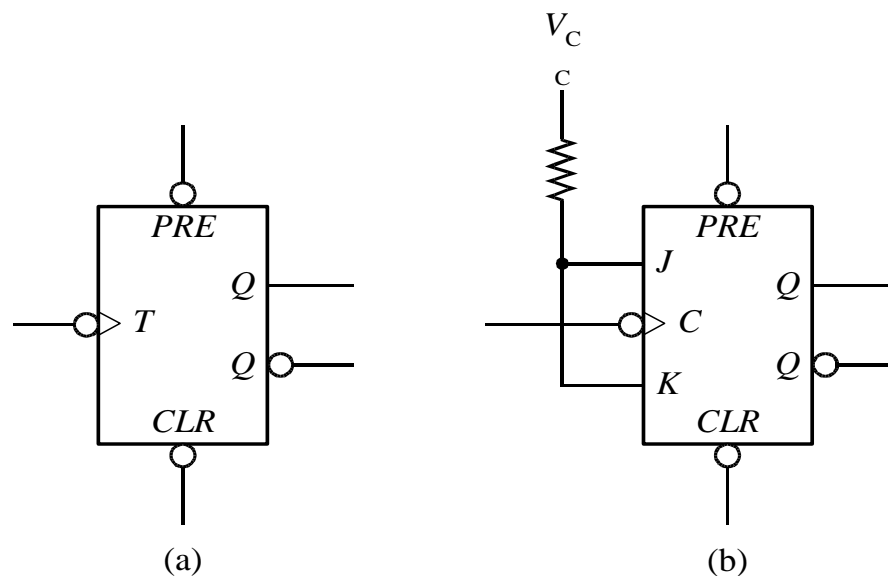


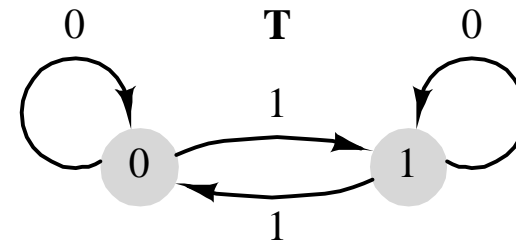
Figure 6.33

6.4 Flip-Flops

➤ Edge-Triggered T Flip-Flop Characteristics

T	Q	Q^*	
↓	0	1	Toggle
↓	1	0	Toggle

(a)



(b)

Figure 6.34

$$Q^* = Q'$$

6.4 Flip-Flops

➤ Clocked T Flip-Flop

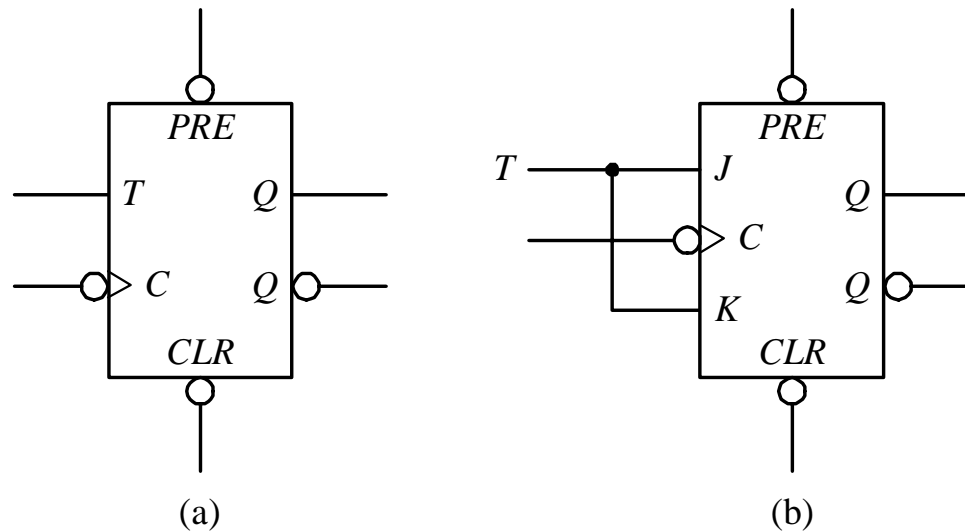


Figure 6.35

6.4 Flip-Flops

➤ Excitation Table for Clocked T Flip-Flops

T	Q	C	Q^*
0	0	↓	0 Hold
0	1	↓	1
1	0	↓	1 Toggle
1	1	↓	0

Figure 6.36

$$Q^* = T'Q + TQ'$$

6.4 Flip-Flops

➤ The Clocked T Flip-Flop Timing Diagram

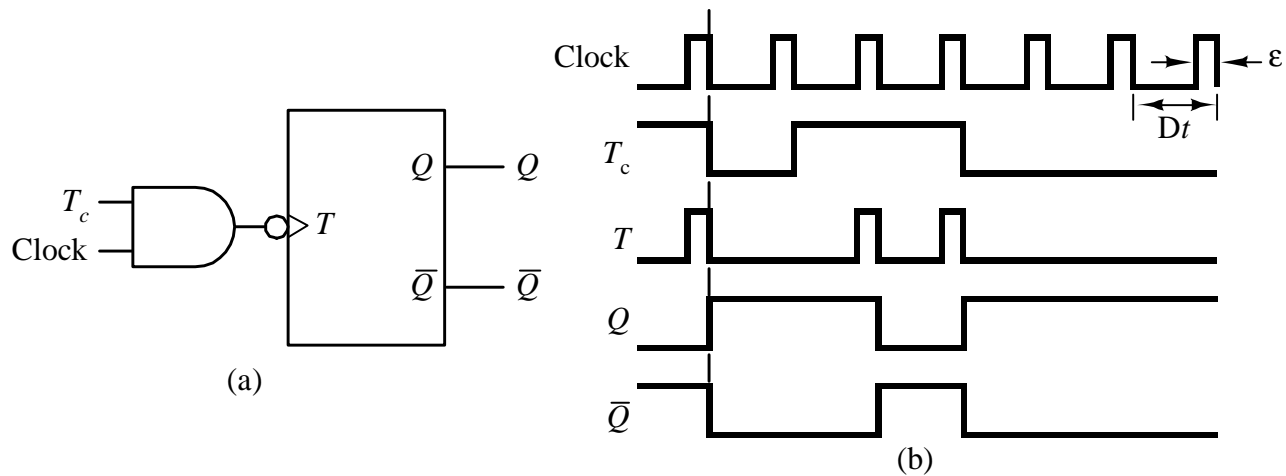


Figure 6.37

6.4 Flip-Flops

➤ Summary of Latch and Flip-Flop Characteristics

TABLE 6.3 SUMMARY OF LATCH AND FLIP-FLOP CHARACTERISTICS

Device	Characteristic Equation
SR latch	$Q^* = S + \bar{R}Q$
Gated SR latch	$Q^* = SC + \bar{Q}R + \bar{C}Q$
D latch	$Q^* = DC + \bar{C}Q$
SR flip-flop	$Q^* = S + \bar{R}Q$
D flip-flop	$Q^* = D$
JK flip-flop	$Q^* = \bar{R}Q + J\bar{Q}$
T flip-flop (edge-triggered)	$Q^* = \bar{Q}$
T flip-flop (clocked)	$Q^* = T\bar{Q} + \bar{T}Q$

6.6 Timing circuits

➤ SE555 Precision Timing Module

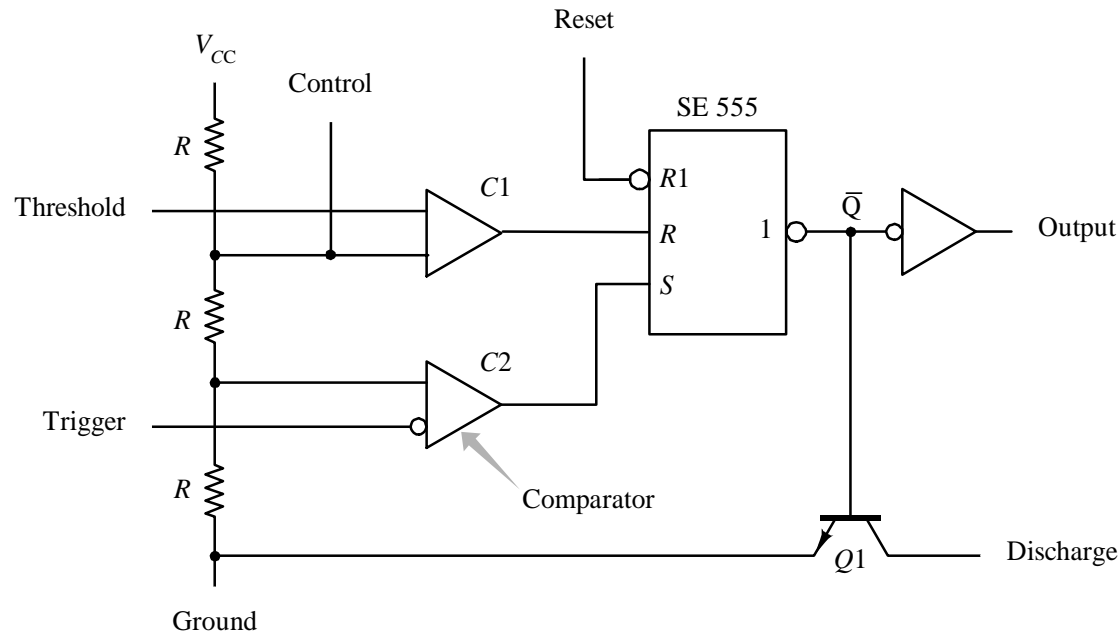


Figure 6.38

6.6 Timing circuits

➤ Astable Operation of The SE555

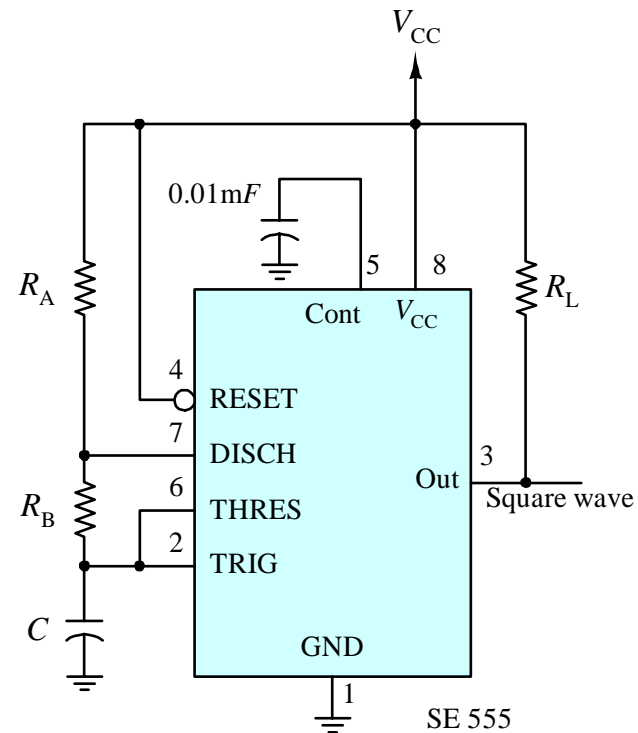


Figure 6.39

6.6 Timing circuits

➤ Monostable (One shot) Device Realization

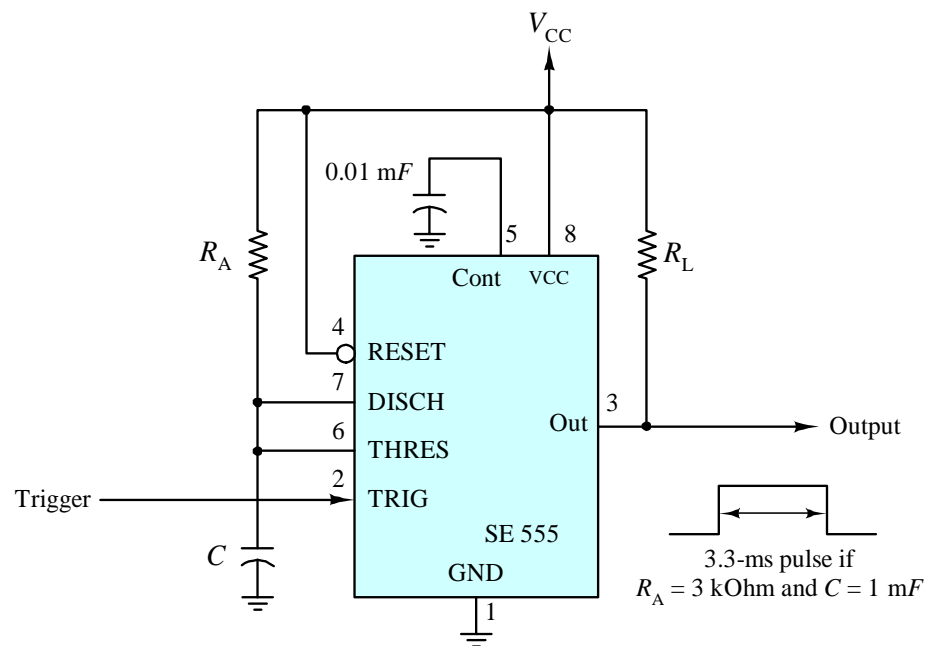


Figure 6.40

6.7 Rapid Prototyping of Sequential Circuits

➤ PROM-based Sequential Circuits

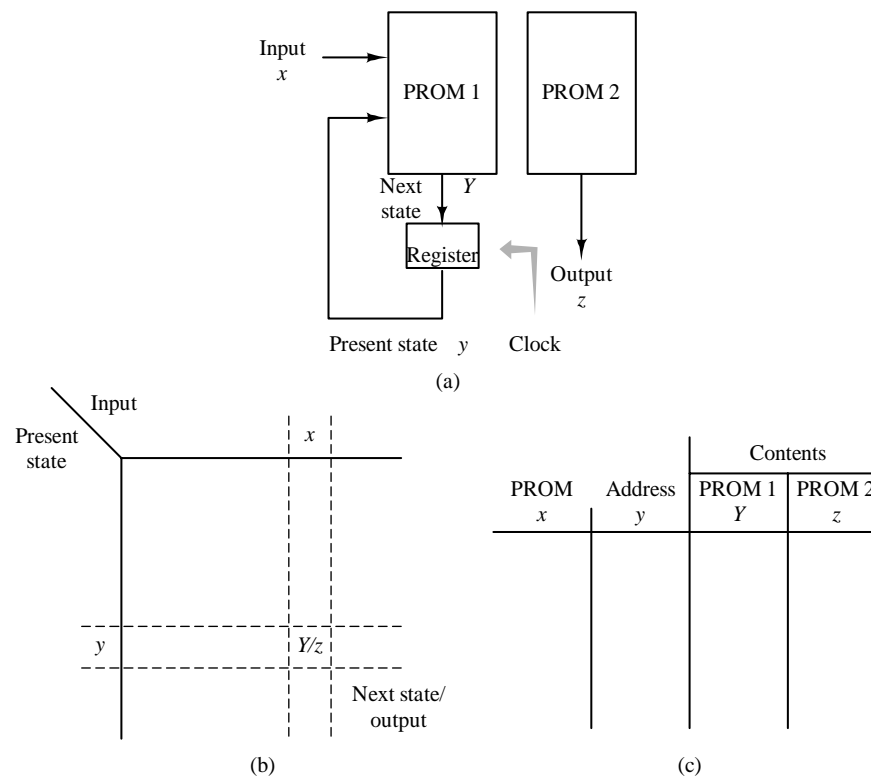


Figure 6.41

6.7 Rapid Prototyping of Sequential Circuits

► PROM-based Sequential Circuit Example

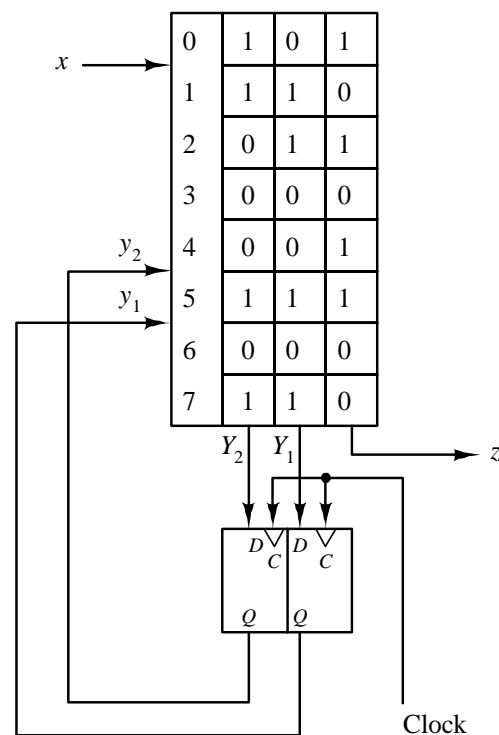
y_2y_1		x	
		0	1
00	10/1	00/1	
01	11/0	11/1	
10	01/1	00/0	
11	00/0	11/0	

 Y_2Y_1/z

(a)

x	y_2	y_1	Y_2	Y_1	z
0	0	0	1	0	1
0	0	1	1	1	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	1	0

(b)



(c)

Figure 6.41

