

In The Name Of Allah

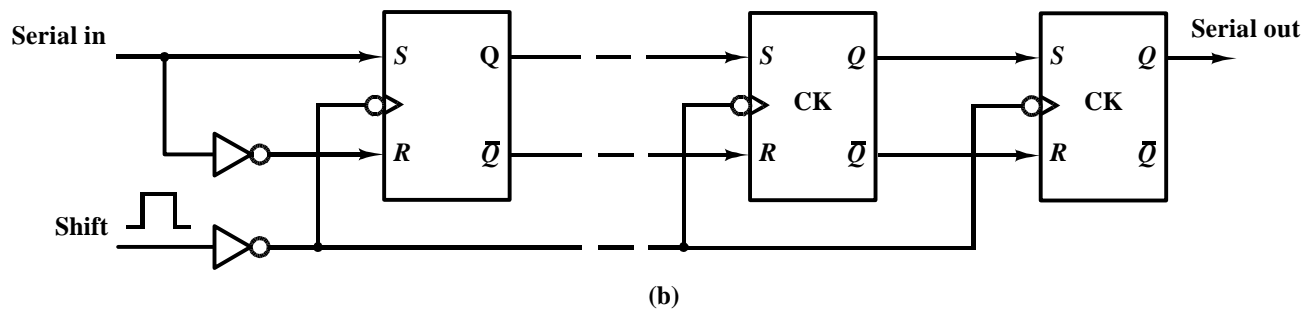
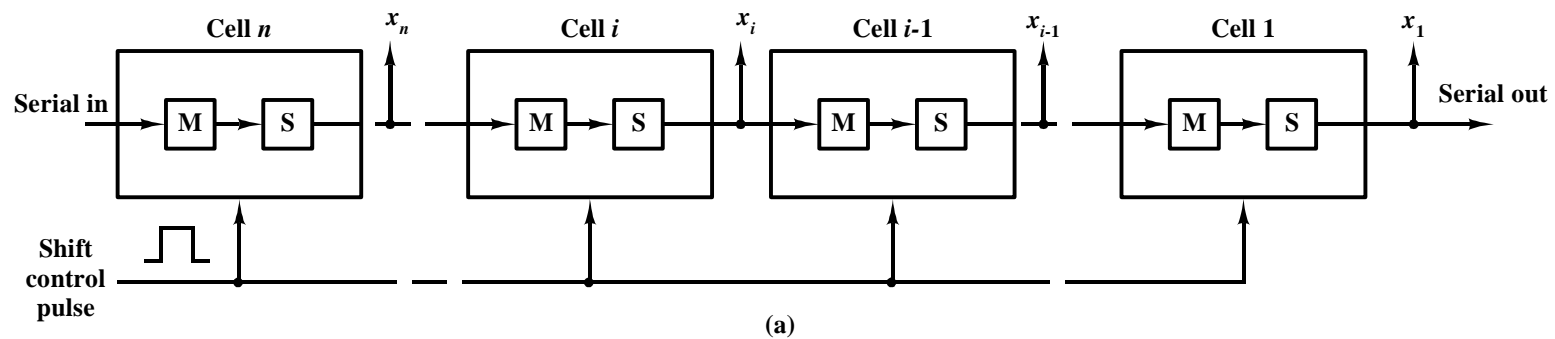
Chapter 7  
Modular Sequential Logic

**Department of Electrical Engineering**

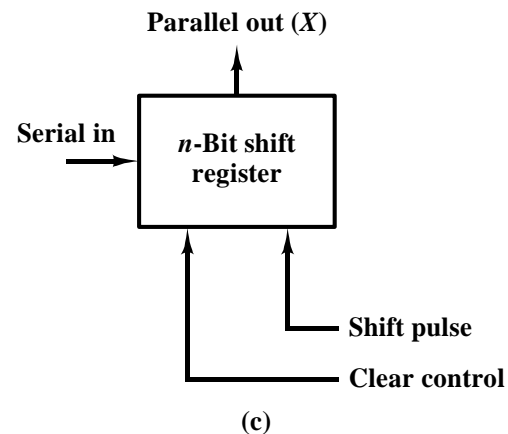
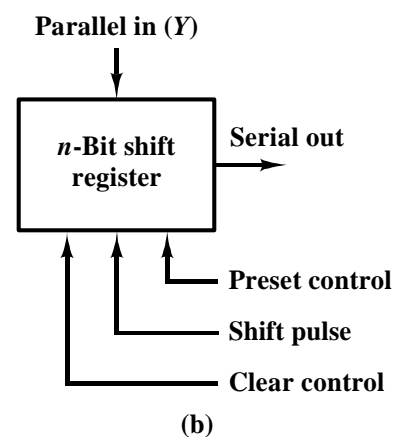
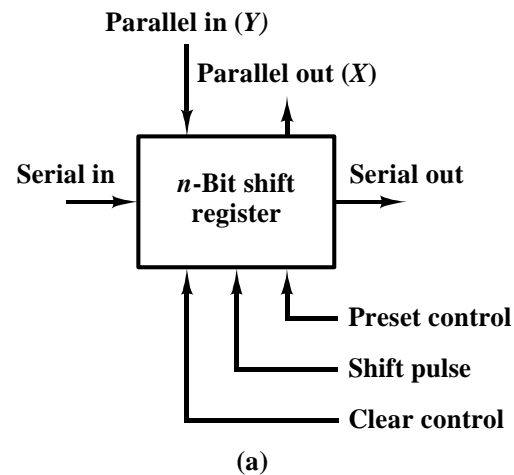
Islamic Azad University

Qazvin Branch

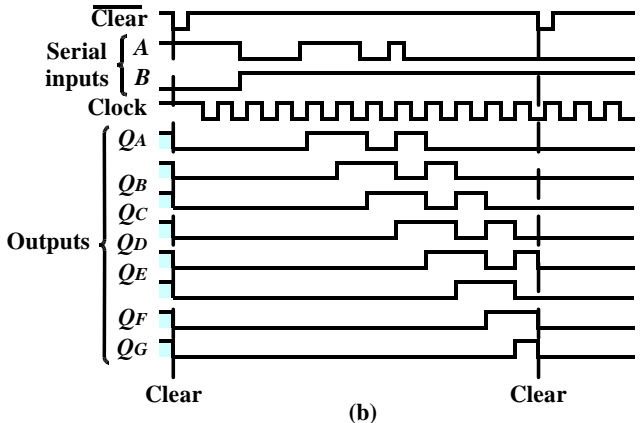
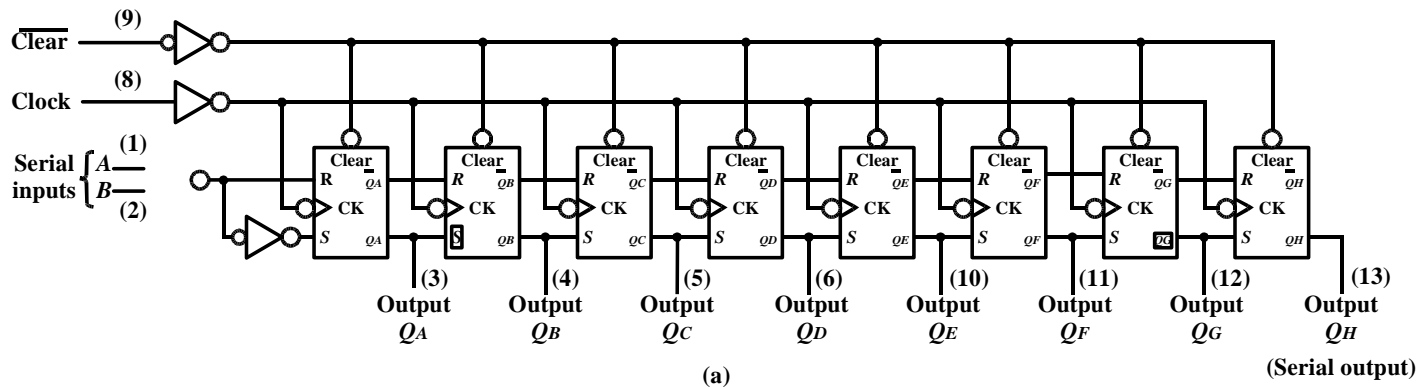
# Serial-in, Serial-out Shift Register



# Generic Shift Register



# SN74164 Serial-in, Serial-out Shift Register

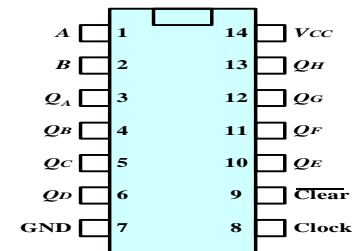


# SN74164 Function Table and Package

Inputs				Outputs			
$\overline{\text{Clear}}$	Clock	A	B	$Q_A$	$Q_B$	$Q_H$	$Q_H$
L	-	-	-	L	L	L	L
H	L	-	-	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$	$Q_{H0}$
H	-	H	H	H	$Q_{An}$	$Q_{Gn}$	$Q_{Gn}$
H	-	L	-	L	$Q_{An}$	$Q_{Gn}$	$Q_{Gn}$
H	-	-	L	L	$Q_{An}$	$Q_{Gn}$	$Q_{Gn}$

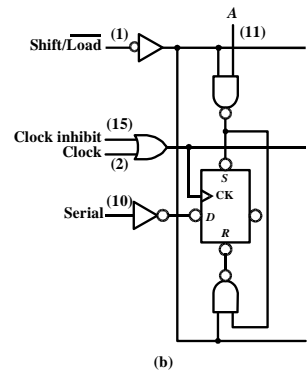
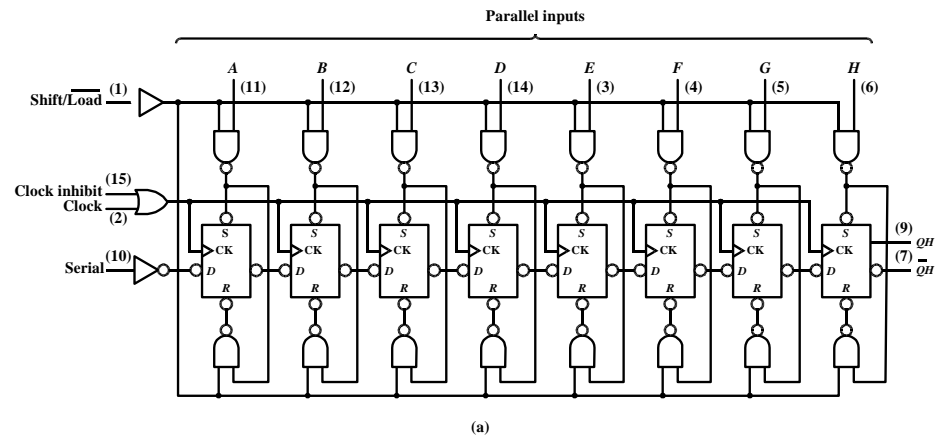
$Q_{A0}, Q_{B0}, Q_{H0}$  = levels of  $Q_A, Q_B, Q_H$ , respectively, before the indicated steady-state input conditions are established.  
 $Q_{An}, Q_{Gn}$  = levels of  $Q_A, Q_G$ , respectively, before the most recent - transition of the clock (1-bit shift)

(c)



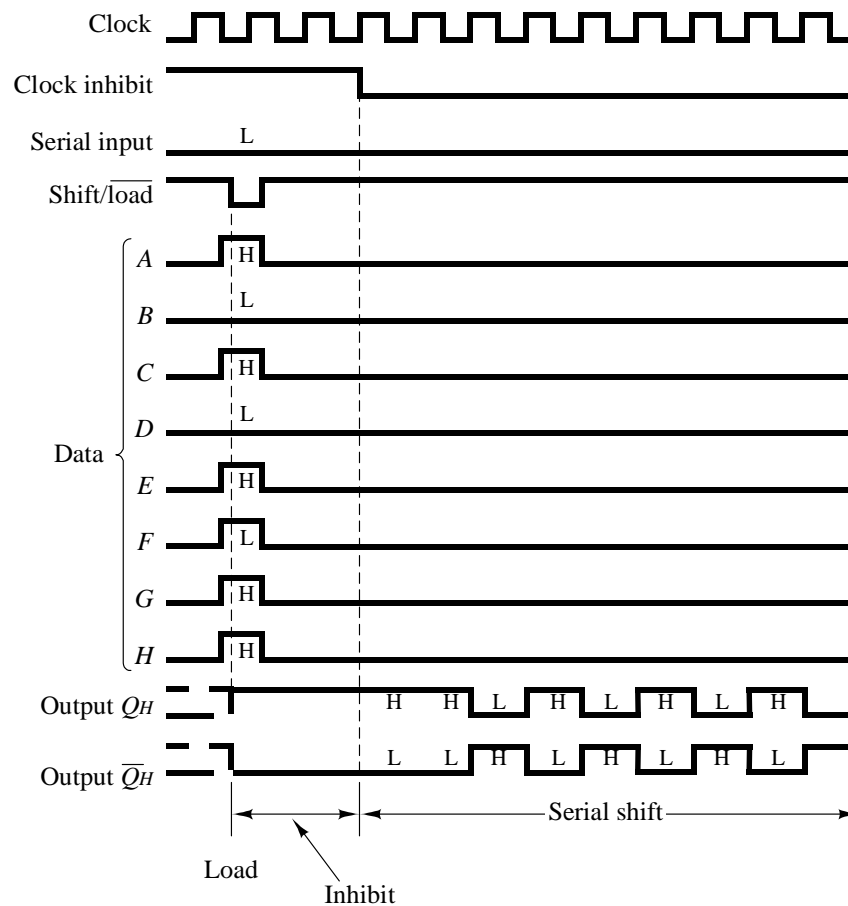
(d)

# SN74165 8-bit Serial-In, Serial-out Shift register



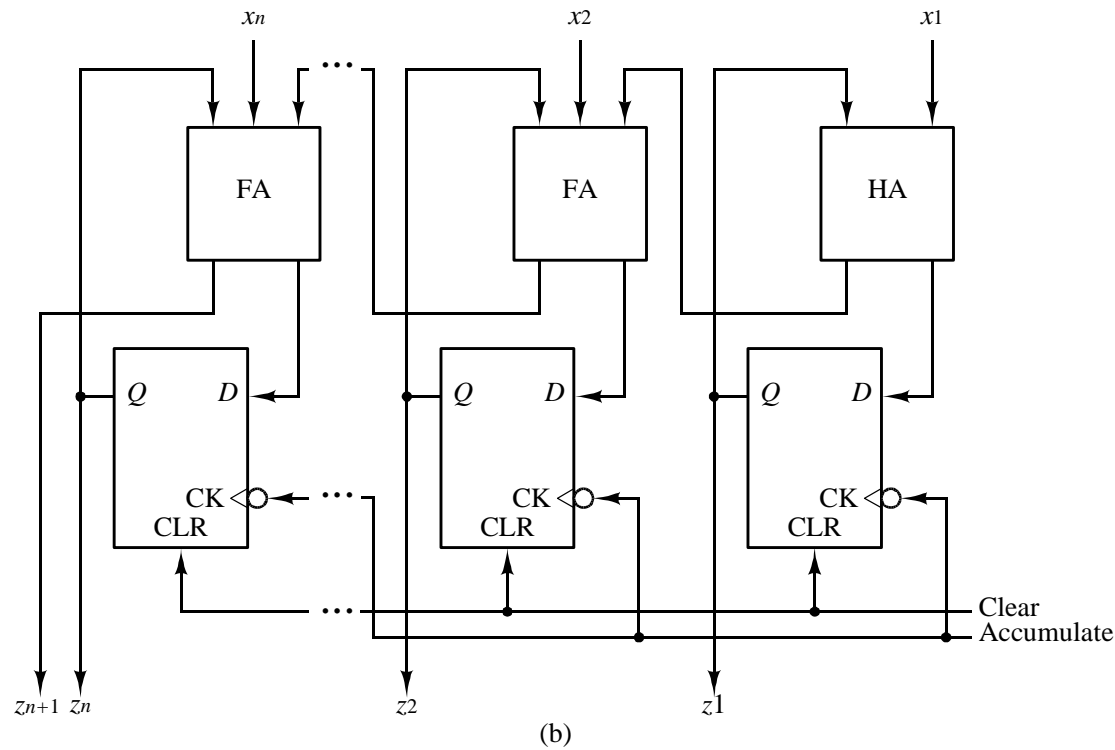
Inputs				Internal outputs		Output
Shift/load	Clock inhibit	Clock	Serial	Parallel A...H	QA QB	QH
L	-	-	-	a...h	a b	h
H	L	L	-	-	QA0 QB0	QH0
H	L	-	H	-	H QA <sub>n</sub>	QH <sub>n</sub>
H	L	-	L	-	L QA <sub>n</sub>	QH <sub>n</sub>
H	H	-	-	-	QA0 QB0	QH0

# SN74165 Timing Diagram

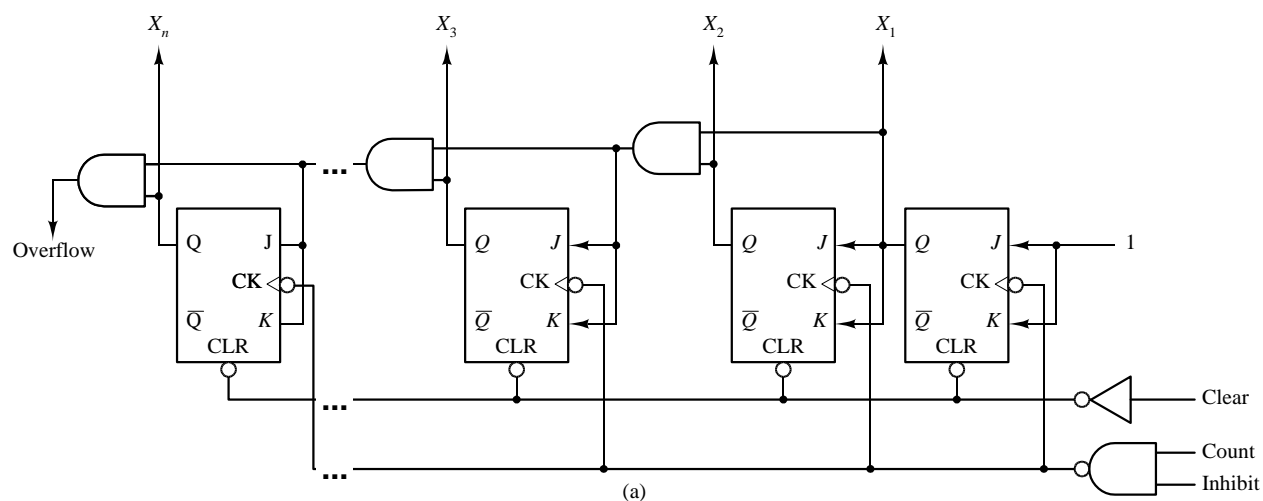


(d)

# Parallel Accumulator



# Synchronous Binary Counter

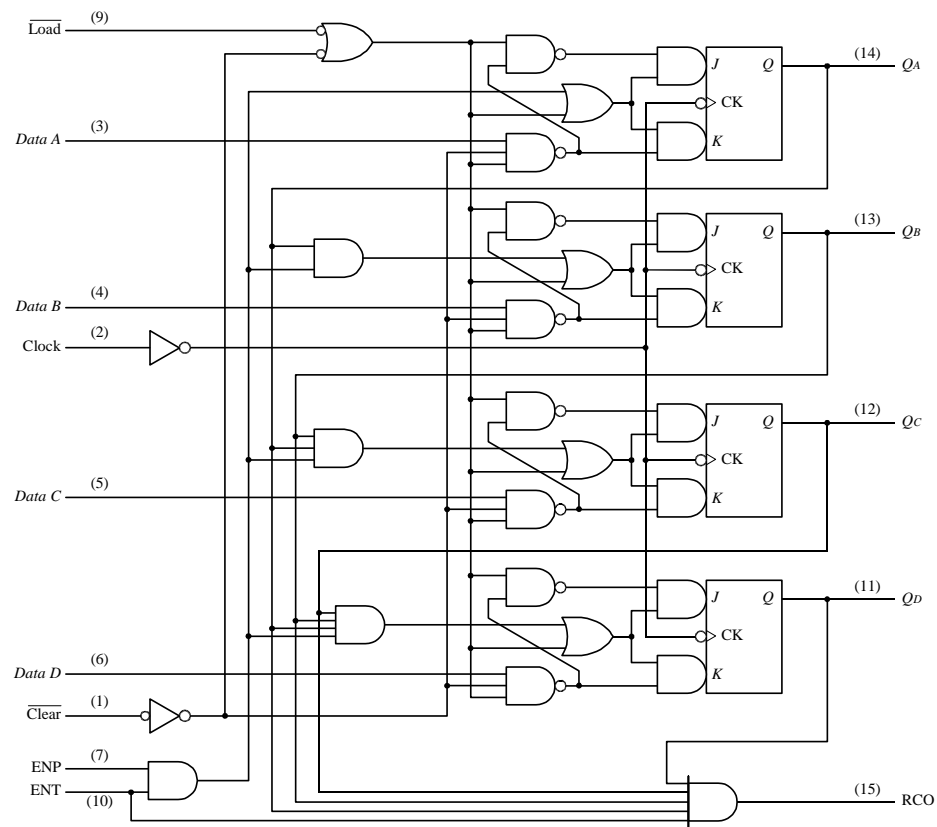


$X_n$	$X_3$	$X_2$	$X_1$
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
1	1	1	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0

← Recycles

(b)

# SN74163 Synchronous Binary Counter

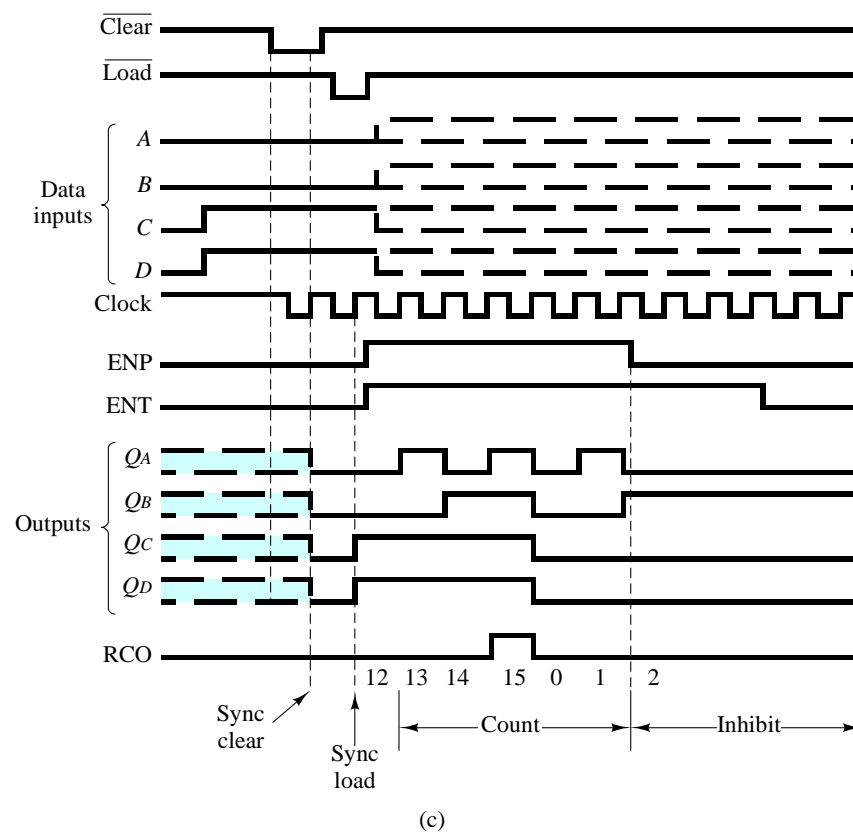


(a)

Inputs				Mode
Clear	Load	ENT	ENP	
L	/	/	/	Synchronous clear
H	L	/	/	Synchronous load
H	H	H	H	Count
H	H	L	x	Hold
H	H	x	L	Hold

(b)

# SN74163 Timing Diagram



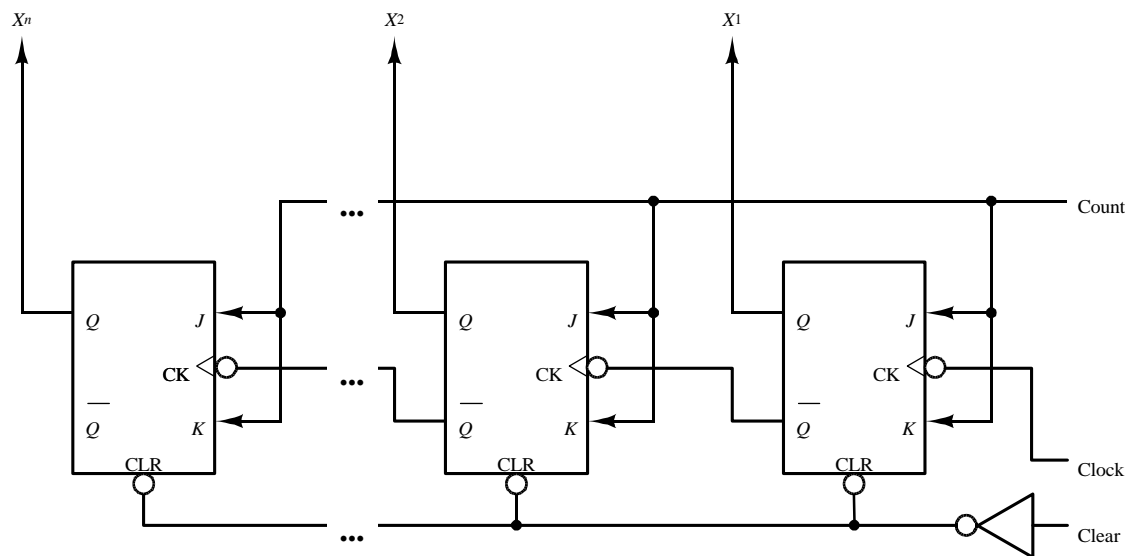
# Asynchronous Down Counter

$X^n$	...	$X^3$	$X^2$	$X^1$		$X^n$	...	$X^3$	$X^2$	$X^1$	
1	...	1	1	1		0	...	0	0	0	
0	...	0	0	0		1	...	1	1	1	
0	...	0	0	1		1	...	1	1	0	
0	...	0	1	0		1	...	1	0	1	
0	...	0	1	1		1	...	1	0	0	
0	...	1	0	0		1	...	0	1	1	

Up count mode

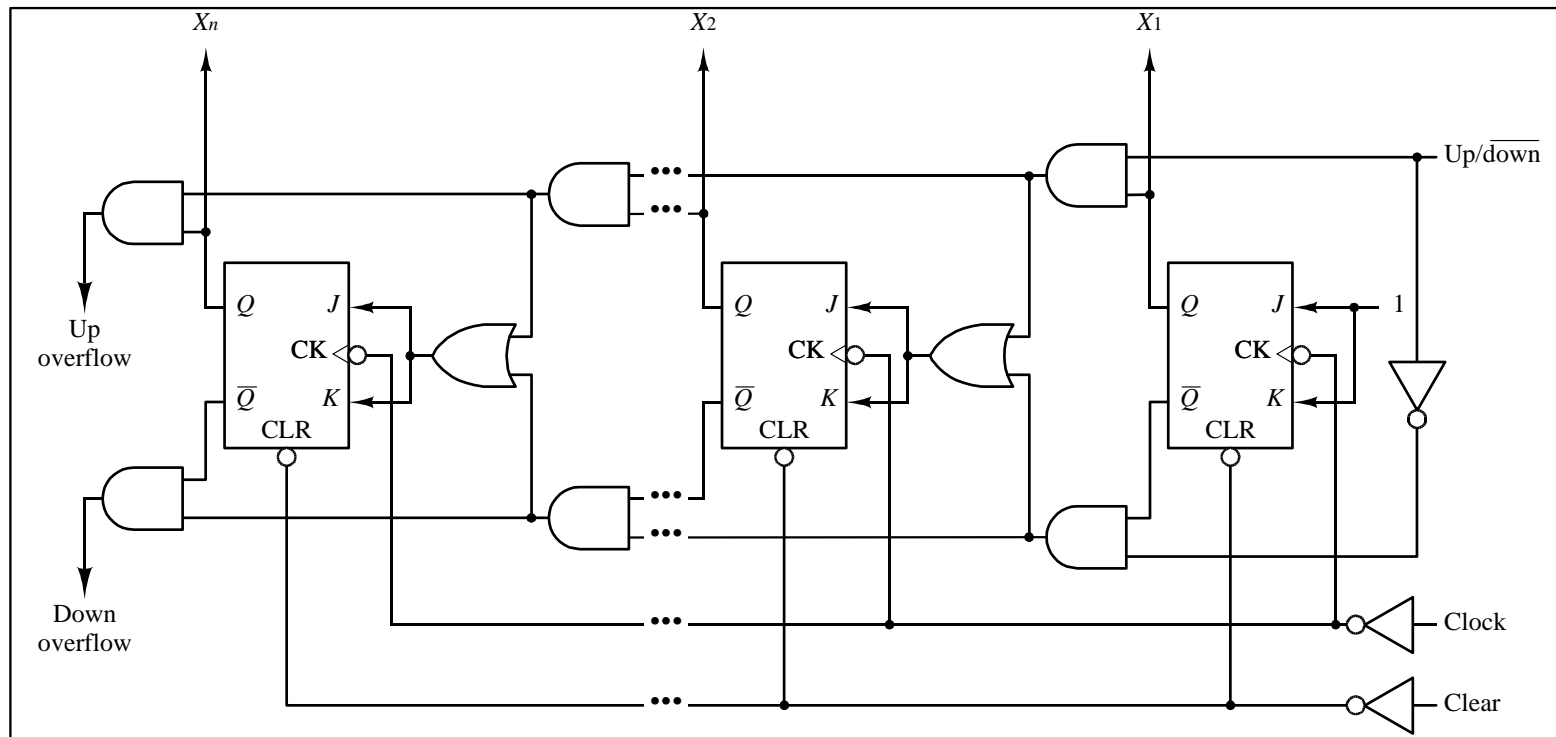
Down count mode

(a)

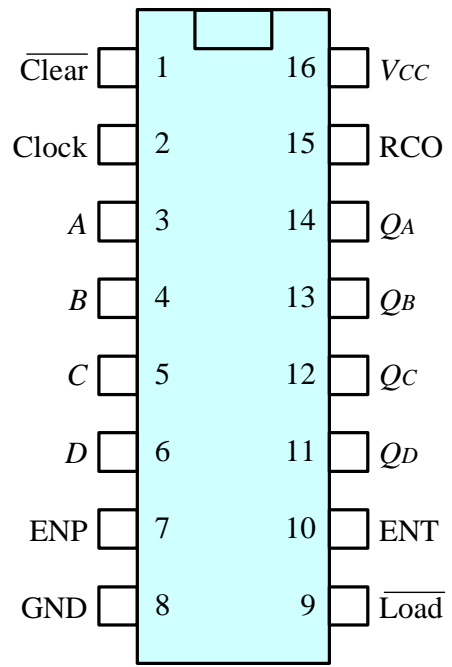


(b)

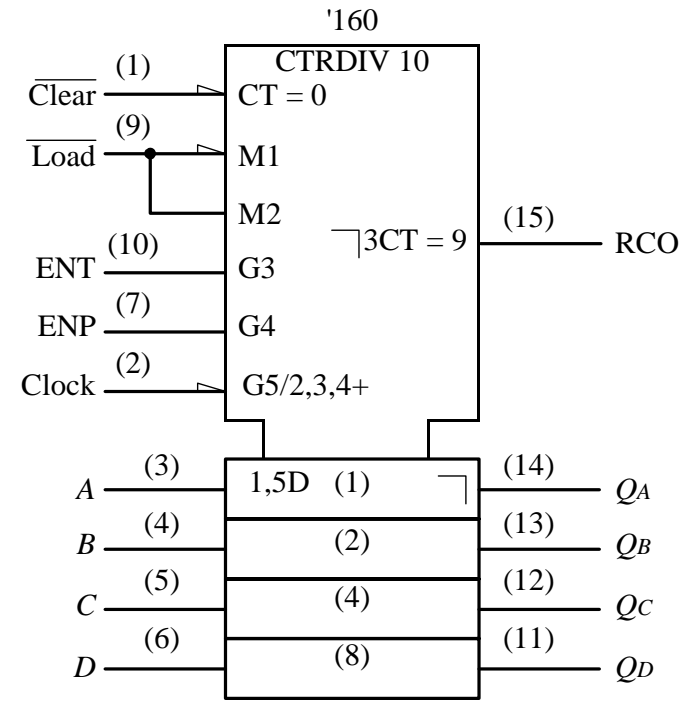
# Synchronous Up/Down Counter



# SN74160 Synchronous Decade Counter

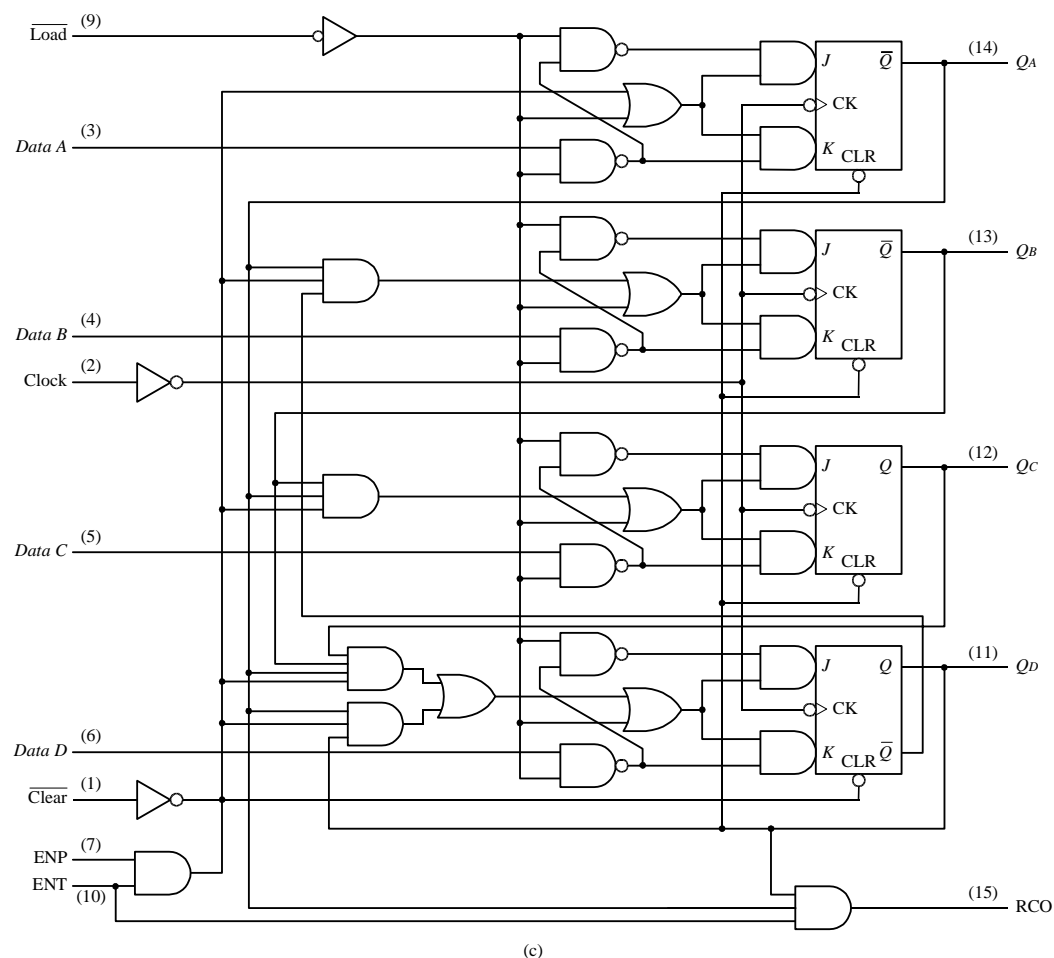


(a)

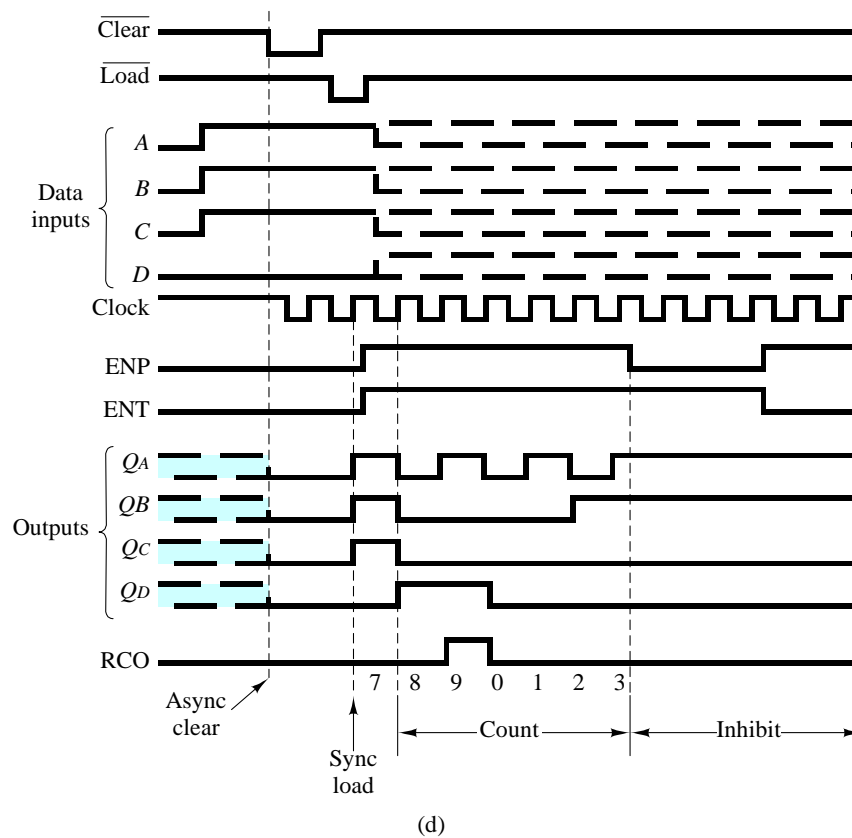


(b)

# SN74160 Logic Diagram



# SN74160 Timing Diagram





# Digital Timer Block Diagram

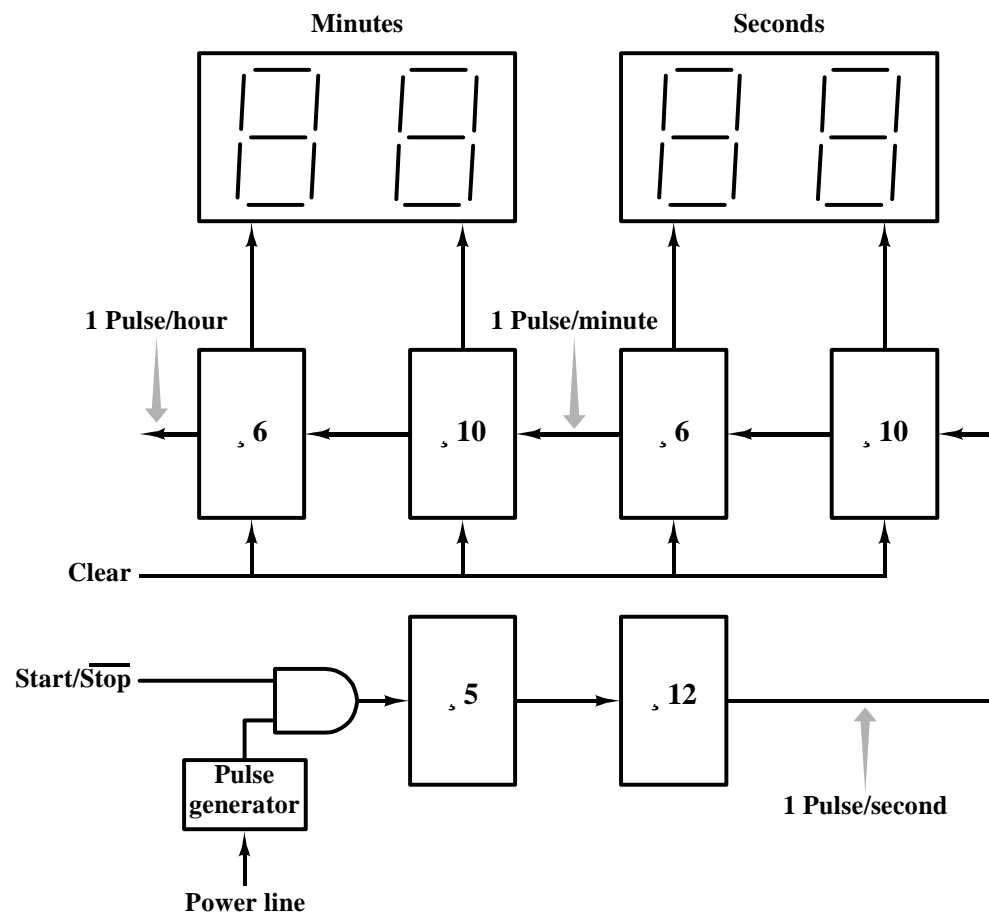
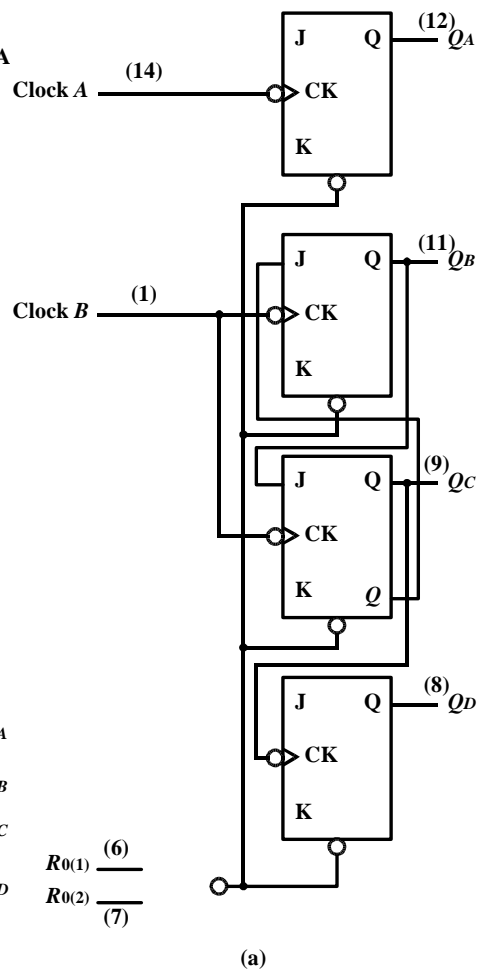
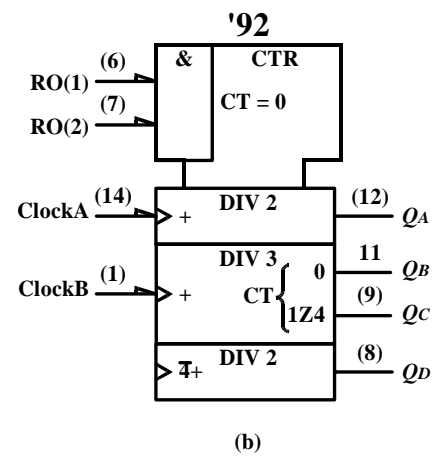
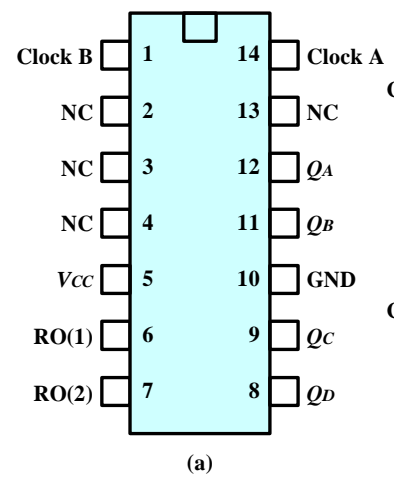
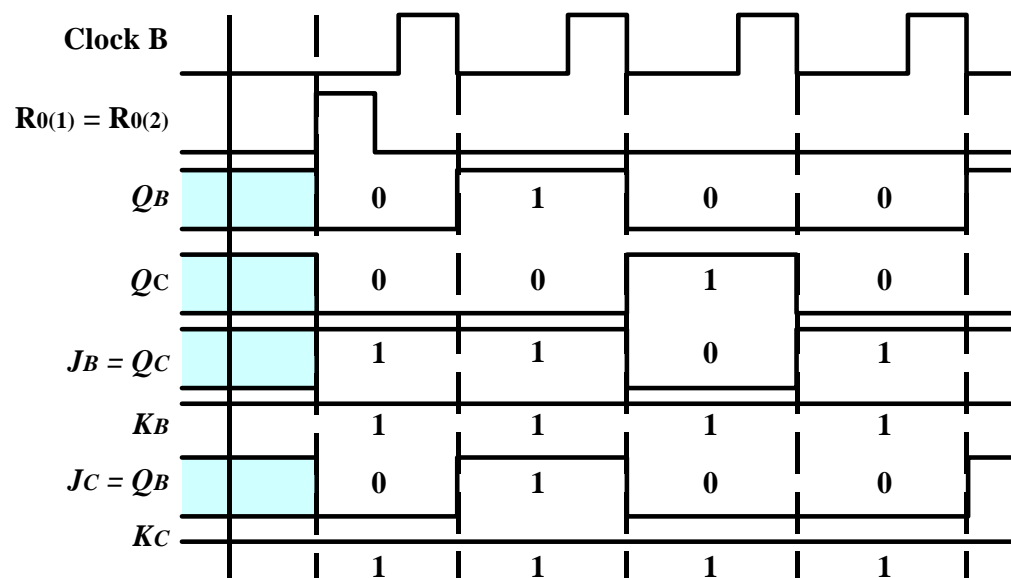


Figure 7.22

# SN7492A Asynchronous Counter

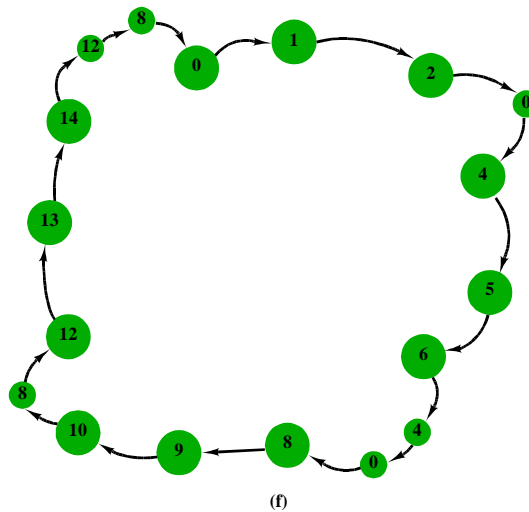
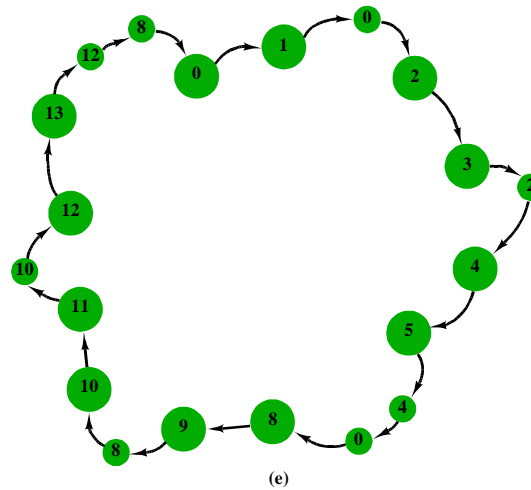


# SN7492A Timing Diagram

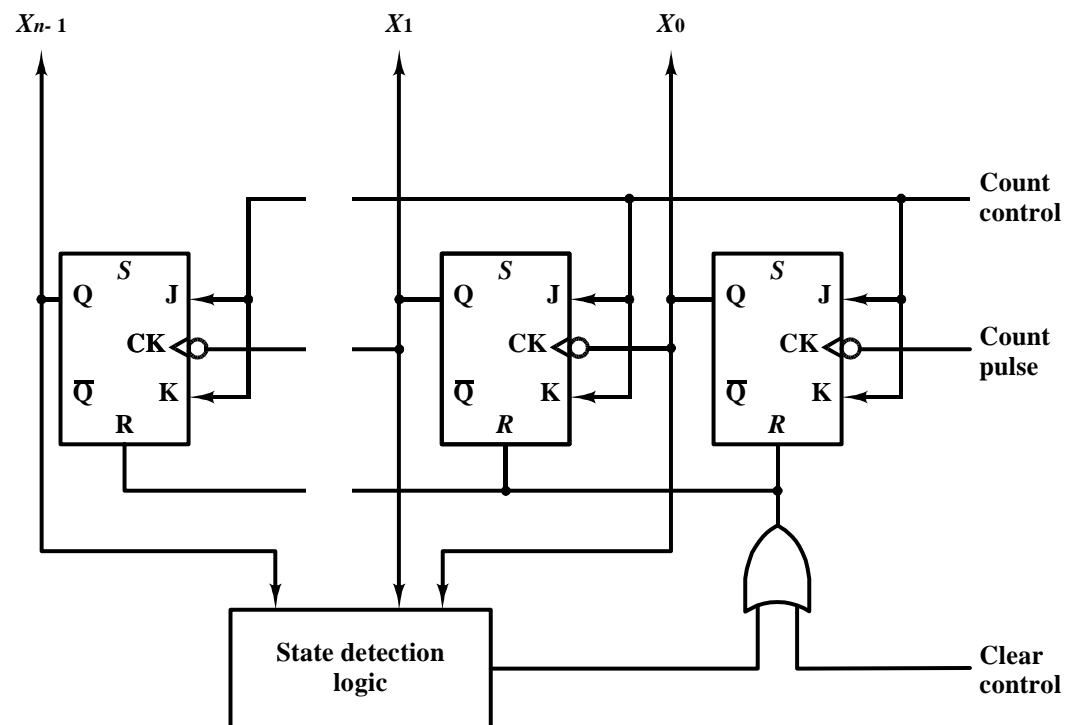


(d)

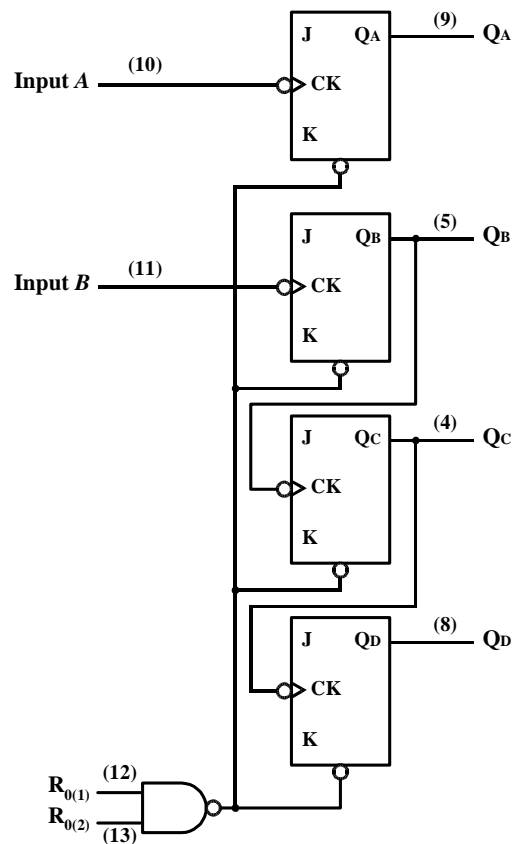
# SN7492A State Diagrams



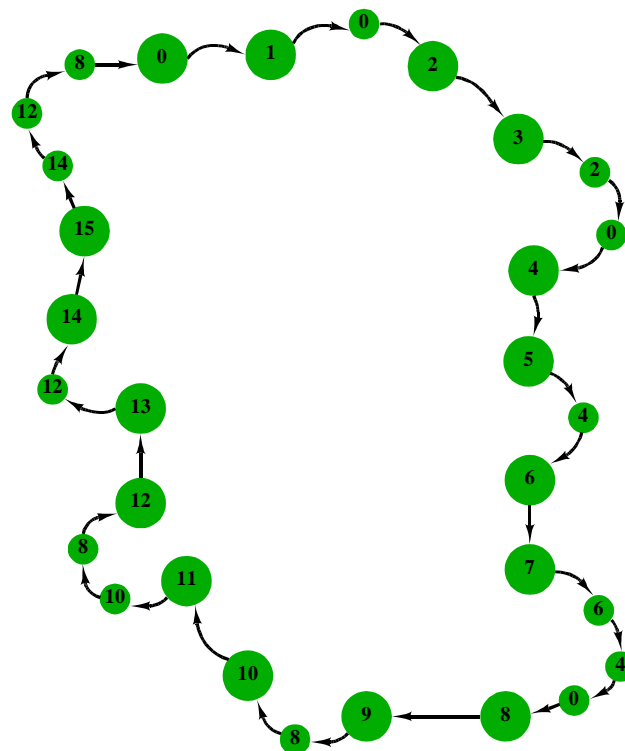
# Modulo- $N$ Asynchronous Counter



# SN74293 Asynchronous Binary Counter

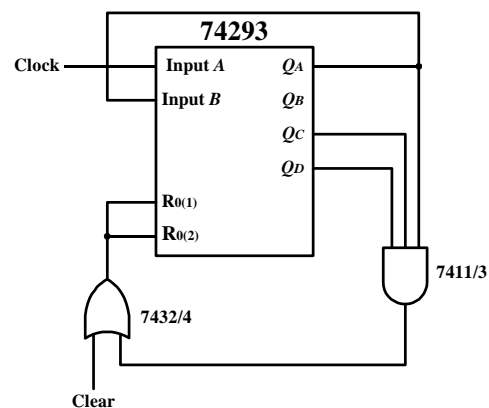


(a)

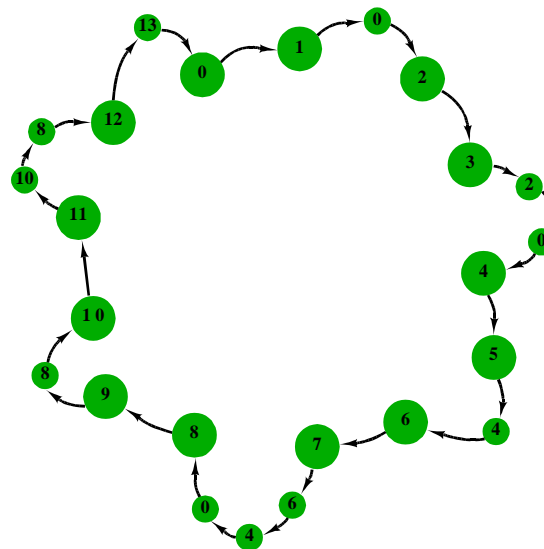


(b)

# Modulo-13 Counter Design -- Example 7.1



(a)



(b)